UM90028

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user manual

NX-DP-GAN039-TSC double pulse evaluation board with top-side cooled CCPAK GaN FETs



Abstract: The NX-DP-GAN039-TSC half-bridge evaluation board enables double-pulse testing of GaN FETs in a top-side cooled copper-clip package (CCPAK). It is optimized for low inductance and features a high bandwidth current shunt that can be used to evaluate the switching performance with maximum precision. In addition, it can be used for thermal investigations and continuous operation up to several kilowatts. This user manual aims to support laboratory setup of the evaluation board and gives and an overview on testing capabilities and typical results.

Keywords: GaN FET, evaluation board, CCPAK, double-pulse, top-side cooling

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1. EVALUATION BOARD TERMS OF USE

The use of the Evaluation Board is subject to the Evaluation Board Terms of Use, which you can find here. By using this Evaluation Board, you accept these terms.

2. High Voltage Safety Precautions

Read all safety precautions before use!

Please note that this document covers only the NX-DP-GAN039-TSC CCPAK double pulse evaluation board and its functions. For additional information, please refer to the Product Specification

To ensure safe operation, please carefully read all precautions before handling the evaluation board. Depending on the configuration of the board and voltages used, potentially lethal voltages may be generated. Therefore, please make sure to read and observe all safety precautions described below.

Before Use:

It is recommended that ALL operation and testing of the evaluation board is performed with the board enclosed within a non-conductive enclosure that prevents the High Voltage supply to be switched whilst open and accessible; see Fig. 1.



Fig. 1. Example of a safety enclosure in the Nexperia lab

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All probes should be positioned before turning on the High Voltage and should be held in place using a suitable probe positioner e.g. PMK MSA100; see Fig. 2.



Fig. 2. Example of a probe positioner

Always use an oscilloscope with protective earth connected.

When probing High Voltage, ensure that the probes have the correct voltage rating / limit.

Ensure that all scope probes are compensated and de-skewed before use, refer to your oscilloscope or probe manual for instructions on how to do this.

If possible, have a visual indicator of High Voltage located close to the evaluation board (LED bar graph or voltmeter) To show when the Bus Voltage (Vbus) and Outputs are at dangerous levels.

Verify that none of the parts or components are damaged or missing.

Check that there are no conductive foreign objects on the board.

If any soldering or modifications are made or carried out, then please ensure that this is done carefully so that solder splashes and debris are not created. Clean the board with Iso-propyl-alcohol and allow it to dry.

Ensure that there is no condensation or moisture droplets on the circuit board, all testing should be carried out within a dry environment without excessive humidity.

If used under conditions beyond the rated voltage and current specification, this may cause defects, failure and or permanent damage.

NEVER handle the evaluation board during operation under ANY circumstances

After use the Nexperia Evaluation Board contains components which may store high voltage and will take time to discharge. Carefully probe the evaluation board once the power has been removed to check that all capacitors have been discharged. You must do this without touching the board except for the multimeter probes that are being used to check.

This evaluation board is intended for use only in High Voltage Lab environments and should be handled only by qualified personnel familiar with all safety and operating procedures. We recommend carrying out operation and testing in a safe environment that includes restricted access only to trained personnel, the use of High Voltage signage at all entrances, safety interlocks and emergency stops and HV insulated flooring.

It should be noted that this evaluation board is intended to be used ONLY for evaluation purposes and should not be used by consumers or designed into consumer equipment in its current form.

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2.1. Warnings

This demo board is intended to demonstrate GaN FET technology. While it provides the main features of a half-bridge converter, it is not intended to be a finished product and does not have all the protection features found in commercial power supplies. Along with this explanation go a few warnings which should be kept in mind:

1. **BE AWARE** there is no specific protection against over-current or over-voltage on this board.
2. If the on-board pulse generation circuit is used in boost mode, a zero input corresponds to 100% duty cycle for the active low-side switch.

3. Introduction

The NX-DP-GAN039-TSC CCPAK double pulse evaluation board enables double-pulse testing of GaN FETs in a top-side cooled copper-clip package (CCPAK). It is optimized for low inductance and features on-board current sensing capability to support typical switching performance evaluation such as switching losses E_{sw}, voltage- and current slopes, reverse-recovery Q_r or gate drive performance directly out of the box. Fig. 3 and Fig. 4 show the evaluation board without the test inductor or heatsink fitted.

The evaluation board can be configured to support both thermal resistance analysis as well as continuous half-bridge converter operation in buck- or boost mode. At a DC input voltage of up to 450 V, output power of up to 5 kW at a switching frequency of 100 kHz can be achieved when paired with a suitable high-power inductor.

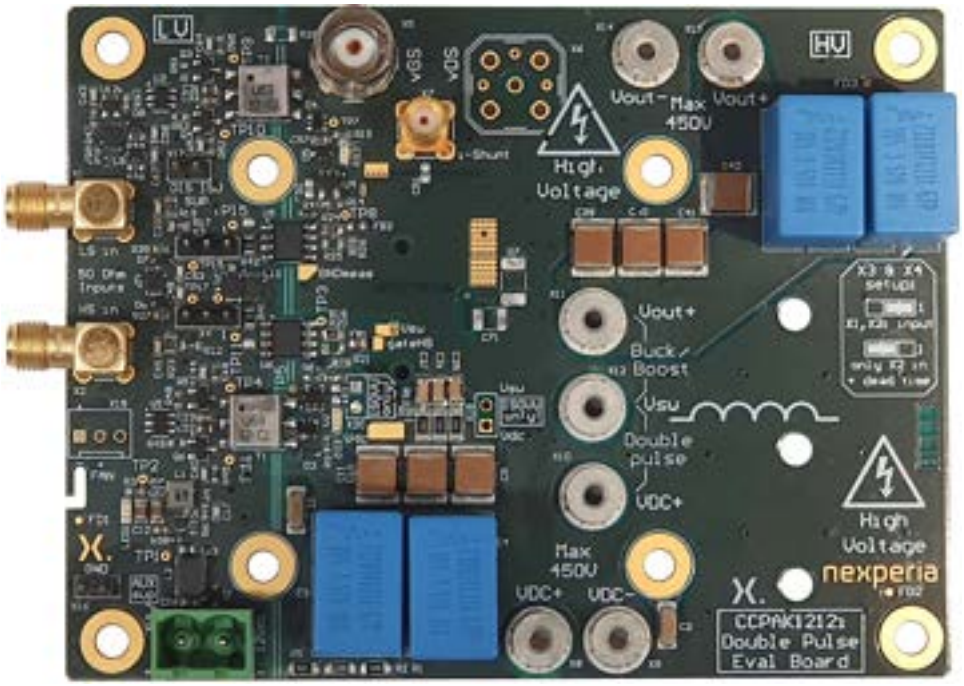


Fig. 3. NX-DP-GAN039-TSC double pulse evaluation board; top view

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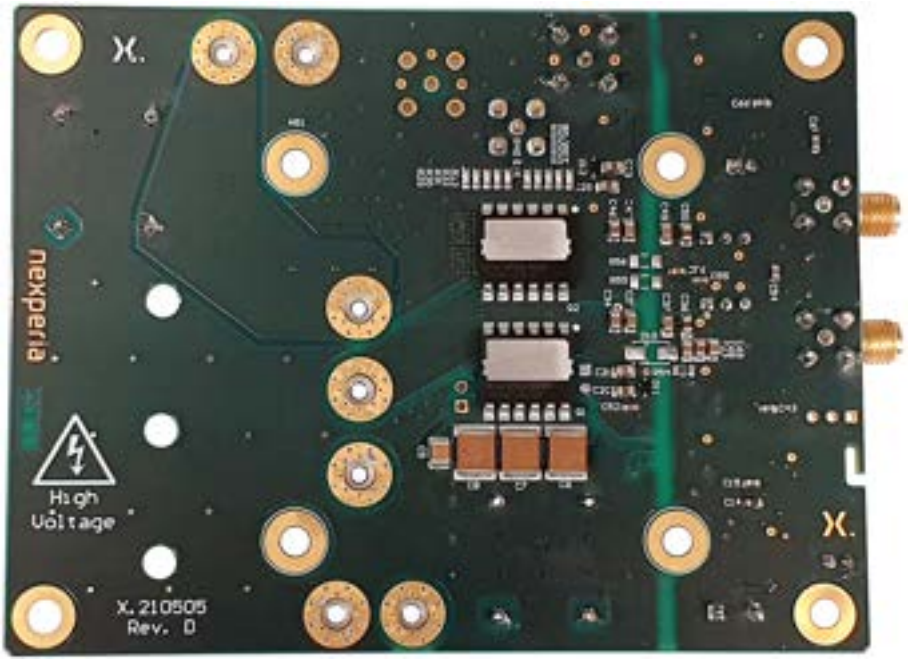


Fig. 4. NX-DP-GAN039-TSC double pulse evaluation board; bottom view (heatsink removed)

3.1. Device overview: GAN039-650NTB 650 V GaN Cascode

The gallium-nitride FET GAN039-650NTB (33 mΩ R_{DSon} typ.) used in this evaluation board is a normally-off device, comprised of a high-voltage depletion-mode GaN HEMT (High Electron Mobility Transistor) combined with a tailored 30 V Si-FET in a cascode configuration.It is assembled as a die-on-die stack for best performance and minimized internal parasitics, housed in a 12-pin 12 mm x 12 mm top-side cooled copper-clip package CCPAK, as shown in Fig. 5.

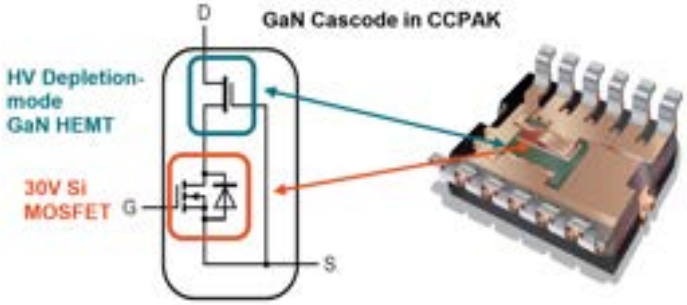


Fig. 5. GaN cascode structure and CCPAK assembly of GAN039-650NTB

Key features of GAN039-650NTB include:

- Very low switching losses
- Rugged gate with high threshold voltage, V_{th} = 4 V, enables single supply gate drive voltage 0 V…10 - 12 V.
- Very good Q_{GD}/Q_{GS} << 1 ratio, protects against parasitic turn-on
- Minimal reverse-recovery
- Very low R_{th} in top-side cooling for SMD
- Best in class third-quadrant off-state conduction performance for wide-bandgap devices
- Very low package inductance (≈1.3 nH @ 100 MHz)

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3.2. Quick reference information

Table 1. NX-DP-GAN039NTB evaluation board Input/Output specifications

Parameter	Value
Input and output voltage	450 VDC max
Junction temperature	150 °C max
Maximum power	Depends on operation conditions, observe T_{case}
Ambient temperature	<50 °C
Auxiliary supply	12 VDC nom., 0.5 A
Logic inputs	Recommended 0 V low, 3.3 V high (5 V tolerant). 50 Ω terminated SMA
Switching frequency	Configuration dependent

Power dissipation in the GaN FET is limited by the maximum junction temperature. Refer to the GAN039-650NTB data sheet.

4. Circuit description

4.1. General description

The circuit comprises a half-bridge circuit featuring two GAN039-650NTB GaN FETs, Q1 and Q2 in Fig. 6. Two high-voltage ports are provided and +HVDC will serve as the input in both double-pulse testing as well as continuous buck converter operation. In buck converter operation, +VOUT will be the output voltage power connection.

With GaN FETs the reverse recovery charge is low and there is no need for additional free-wheeling diodes. Due to this, the capability of the half-bridge is bi-directional and the +VOUT node can also be used as the input for boost converter operation if desired. In all cases one GaN FET acts as the active power switch while the other carries the free-wheeling current. During the free-wheeling phase, the conducting device may be enhanced as a synchronous rectifier via its gate and there is no need for external free-wheeling diodes.

Two input connectors are provided which can be connected to sources of logic-level command signals for the hi/lo gate driver. Both inputs X1 and X2 may be driven by off-board signal sources, or alternatively, a single signal source may be connected to an on-board pulse-generator circuit which generates the two non-overlapping pulses with fixed dead-time. Jumpers X3 and X4 determine how the input signals are used.

An inductor is provided as a starting point for double-pulse investigation. This is an approx. 18 µH toroid intended for device testing in double-pulse with stable inductance up to 40 - 50 A.

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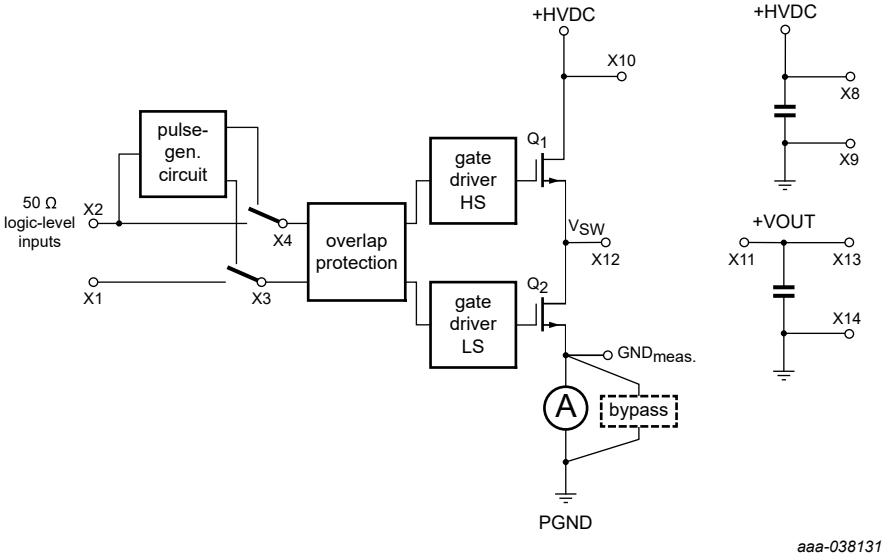


Fig. 6. NX-DP-GAN039-TSC CCPAK evaluation board functional block diagram

4.2. Circuit setup for double-pulse testing

In order to use the test platform for its main purpose, which is the double-pulse switching evaluation of GAN039 in CCPAK, it is recommended to use the configuration as shown in Fig. 7. In this setup, the low-side FET Q2 is the active device and receives its gate inputs directly from a function generator through the SMA connector X1 while the other signal input X2 can be left open or kept low. The jumpers X3 and X4 should be set to connect pin 1 and 2, as indicated on the silkscreen. The test inductor is connected between the switch-node V_{SW} and the HV input voltage and Q1 serves as the free-wheeling device.

The board contains fixed access nodes for measurement of the gate-source voltage V_{GS}, drain-source voltage V_{DS} and source current, I_S of the low-side FET Q2. The reference potential for these measurement is the GND_{meas} node at the source potential of Q2, which is different from PGND. Therefore, a HV supply with galvanically isolated outputs must be used in order to capture precise waveforms. An oscilloscope with a bandwidth of at least 1 GHz and high-frequency passive probes are recommended to use with this circuit in order to capture all necessary details of the switching transitions at the low-side.

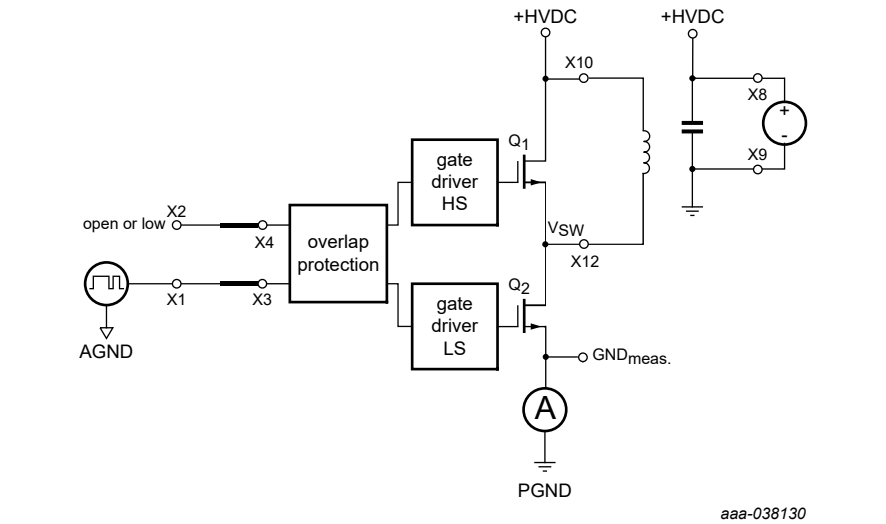


Fig. 7. Setup for double pulse testing

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4.3. Circuit setup for continuous operation

For continuous operation of the GAN039-NTB(A) CCPAK double pulse evaluation board, some important modifications compared to the double pulse test are required, as shown in Fig. 8 for buck-converter operation:

- A HV DC-source and DC-load with sufficient power rating has to be used for continuous operation.
- The current sensor must be bypassed with a low impedance solder connection to prevent damage to the sensor.
- A test inductor with sufficient current handling and high-frequency capability must be attached between X12 and X11. The included test inductor for double-pulse evaluation is not suited for continuous operation.
- Both single-input (jumpers X3 and X4 connect between pin 2 and pin 3) and dual-input (jumpers X3 and X4 to connect pin 1 and pin 2) mode can be used for continuous operation. Single-input uses X2 signals only and creates an inverted signal for synchronous rectification with fixed dead-time between pulses. In dual-input mode, both input connectors can be used independently to experiment with dead-time setting or to turn-off synchronous rectification. In either case, the board has an overlap-protection circuit that prevent both gates being pulled high at the same time.

CAUTION: Bypassing the SMD current sensor is mandatory for continuous operation to not exceed the 2 W power rating of the shunt array. Failing to do so may destroy the sensor. Also please use the included inductor for pulsed-testing only.

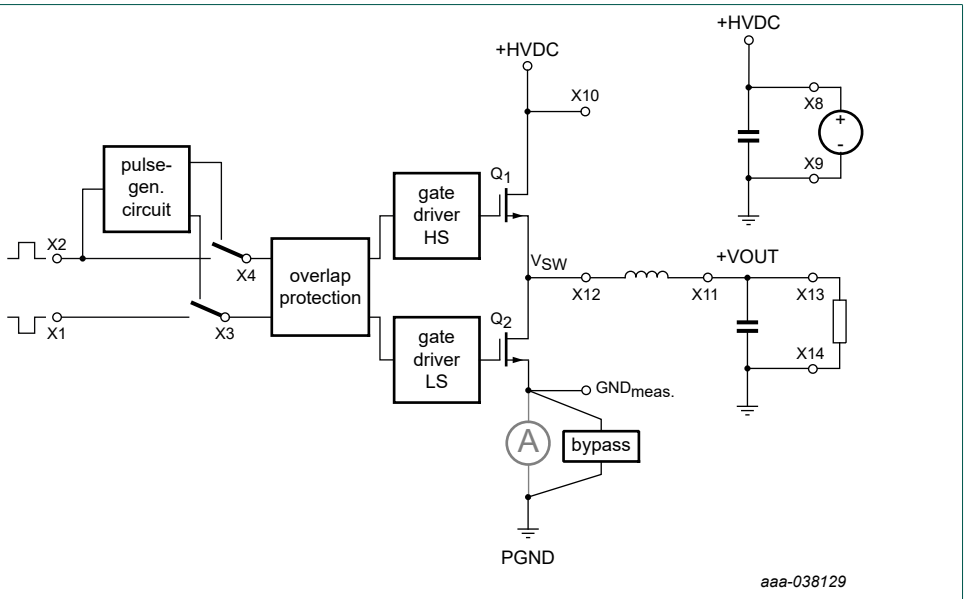


Fig. 8. Setup for continuous buck converter operation

4.4. Description of circuit sections

Input section

- Power ports: The power ports to attach the input and output HV connectors as well as the test inductor are M3 screw terminals. It is recommended to not exceed 32 A RMS current at these ports.
- AUX-Supply: All the auxiliary circuitry on the isolated low-voltage side as well as the FAN will be supplied through the 5.08 mm connector X15. The nominal input voltage of 12 V should not be exceeded to not damage the attached FAN. It can be lowered down to 5 V to reduce FAN speed if desired. Three green signal LEDs will indicate when the supply voltage levels are

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sufficient: LED1 for the LV input side, LED2 for the high-side gate supply and LED3 for the low-side gate supply.

- Signal inputs: The SMA connectors X1 and X2 are terminated with 50 Ω resistors to be connected with standard function generators. Recommended driving voltage is 0 V-3.3 V but the inputs can tolerate 5 V if unavoidable. Jumpers X3 and X4 control whether both signal inputs are forwarded to the overlap protection circuit or whether X2 acts as the sole input source. In the latter case, an inverted pulse signal with fixed dead-time of approx. 80 ns is created on the board. Please note that when using single input mode, one device will always be actively turned-on outside of the dead-time intervals. The dead-time duration can be changed by modifying R27 (delay of HS rising edge) and R39 (delay of LS rising edge). It is always recommended to check signal integrity after such a modification to avoid unexpected device behavior.

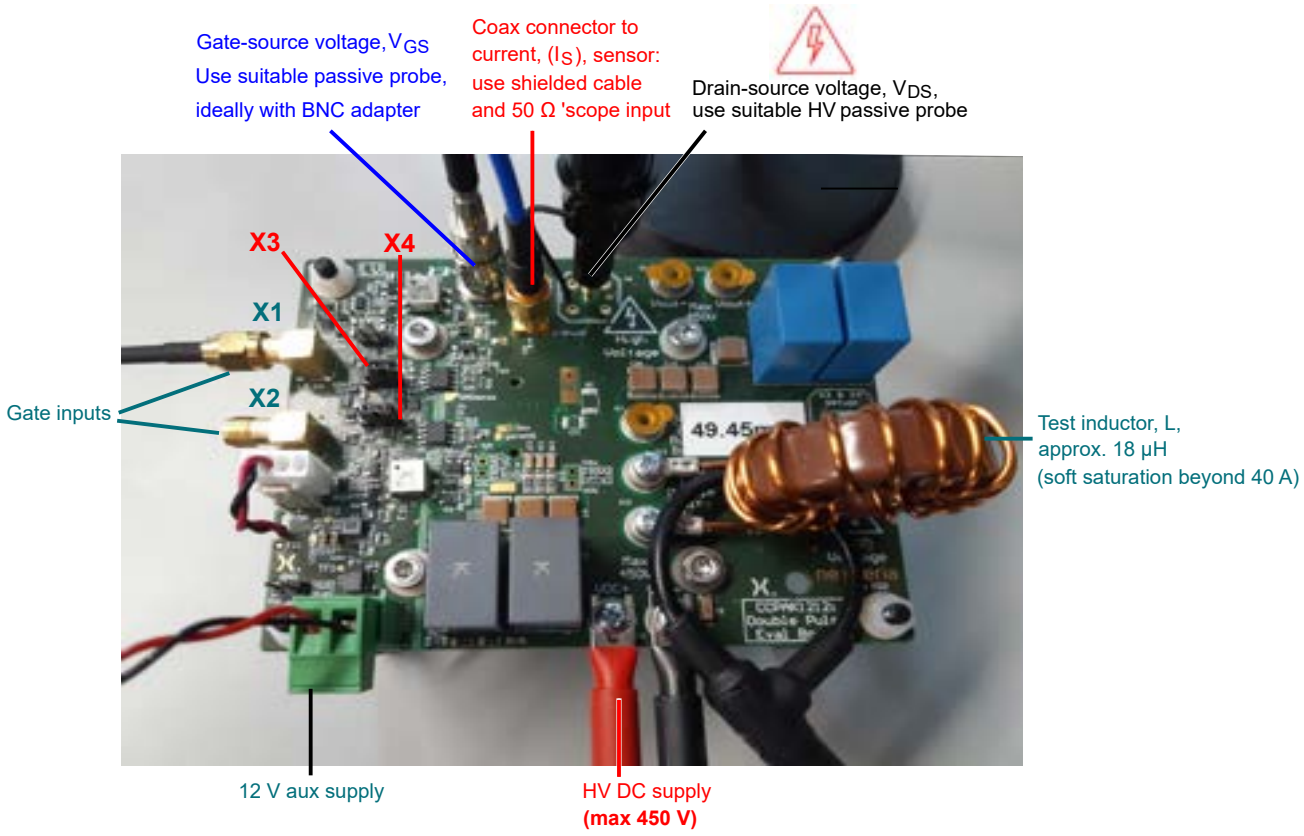


Fig. 9. Evaluation board setup in double pulse configuration with probes attached

In front of the gate drive inputs, an overlap protection circuit formed by XOR and AND gates U8 and U10 ensures that the gate drivers do not receive turn-on signals at the same time. Nevertheless, depending on the gate resistance and due to different delays in turn-on and turn-off speed of the GaN FETs, minimal cross conduction might still occur when two logic-high signals are sent.

The overlap protection circuit is intended to protect the circuit against unwanted cross conduction. For some investigations on thermal resistance R_{th}, it can be helpful to turn both devices on at the same time in order to conduct DC current through both FETs at the same time. In this exceptional case, the overlap-protection can be defeated by re-soldering resistors R41 and R42 to connect the gate driver inputs directly to the supply voltage, (see Fig. 26). **IMPORTANT: only use this mode at very low voltage and revert to the original state before doing any other measurements to protect the circuit.**

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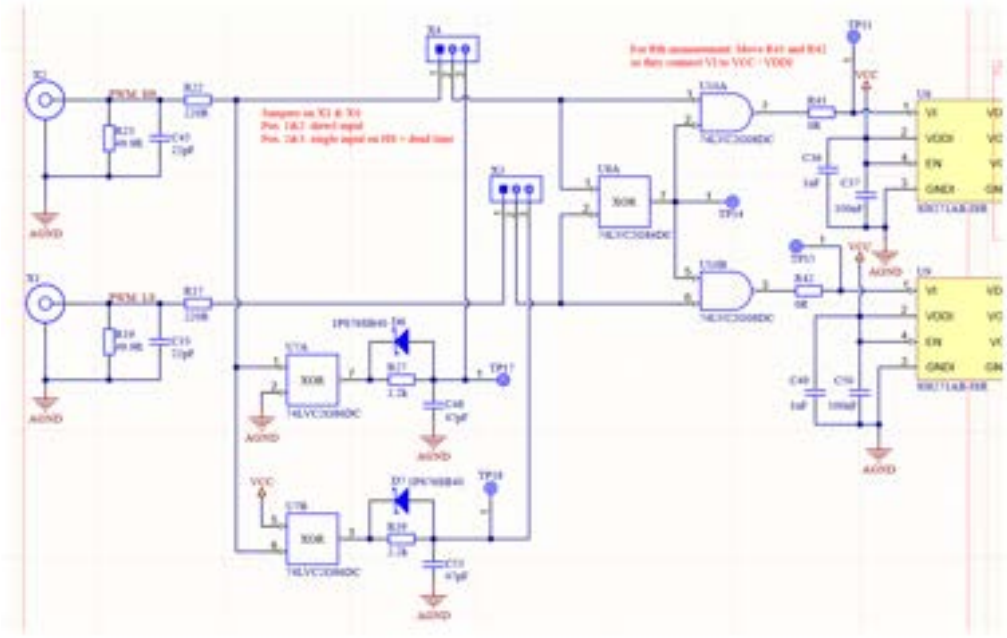


Fig. 10. Signal input section

Gate driver supply

The board is equipped with two identical push-pull power supplies to supply the low-side and the high-side gate driver and ensure galvanic isolation. In series to them, adjustable linear regulators are utilized to stabilize the supply voltage for both gate drivers. In the standard setting, the GaN FETs will be turned on at +12 V and turned off at 0 V. Negative turn-off voltage is not required for these devices since they have high threshold voltage and very user friendly Q_{GD}/Q_{GS} << 1 ratio. For fast switching GaN-FETs, minimizing the parasitic capacitance of the power supply is mandatory for stable operation and the input to output capacitance of the selected push-pull transformers in this layout are rated at <1 pF.

While the fully isolated gate supply is best for maximum flexibility in testing, a lower BOM cost alternative can be the bootstrap high-side supply. In order to modify the board for bootstrap supply, the isolated supply must be disabled by adding a jumper at X17 and footprints R55 and R56 should be bridged, for example with 0 Ω 1206 resistors. A very fast bootstrap diode with low reverse-recovery and minimal diode capacitance (e.g. PNU65010ER) should be selected. When using the bootstrap supply setup, the AUX input voltage (X15) is proportional to the gate driver supply voltage and might be reduced for evaluation. It should be noted that this will also change the FAN speed at the attached heatsink.

CAUTION: do not populate the bootstrap diode D10 when running the isolated gate supply and to disable the push-pull supplies through connection of X17 when operating as bootstrap circuit.

Gate circuitry

The gate drive circuit consists of two individual gate resistors that permit individual turn-on and turn-off optimization. In series, a ferrite bead is fitted to ensure good switching behavior in all operation scenarios. In the original state, 15 Ω gate resistors with increased power rating are equipped in series to a 30 Ω @100 MHz (BLM18PG300SN1D) ferrite bead.

Resonance damping network and snubber

It is always recommended to use multi-layer ceramic capacitors (MLCCs) in combination with fast GaN devices in order to minimize power loop inductance. Due to the very low equivalent series

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resistance (ESR), the DC link capacitance might have very low damping in the MHz range, leading to unnecessarily prolonged ringing after switching events. The parallel resonance damping network (R11-13, C25-27) helps to improve behavior without increasing loss.

The RC Snubber (R7, C71) is not populated on the board and typically not required for GAN039 in normal conditions.

Measurement section

The evaluation board offers fixed measurement nodes for reliable and repeatable measurements of the gate-source voltage V_{GS}, drain-source voltage V_{DS} and the source current I_S of the low-side GaN FET. These are optimized to give precise waveforms while being quick and easy to set up. Ground reference of all these measurements is the source potential of the low-side GaN FET, named GND_{meas}.

The V_{GS} node (X5) is pre-equipped with a BNC connector and is best to be used with a common BNC tip adapter on a passive probe. For V_{DS}, a similar HV node (X6) is available but the BNC adapter is not populated as most adapters are not specified for HV operation. An easy alternative is to use the provided through-hole pads to attach the spring tip accessory of a high-voltage probe.

For evaluation of I_S, connection to the high bandwidth SMD shunt current sensor (X7) is available through an SMA connector. The SMD shunt consists of ten 470 mΩ resistors in parallel, leading to an effective total resistance in the range of 47.5 mΩ and a power handling capability of 2 W. It is recommended to use a high quality, double shielded SMA to BNC coaxial cable for connection of the sensor to the 50 Ω input of the oscilloscope. Since the reference of the voltage reading is the source potential of the GaN FET, the current will appear inverted on the oscilloscope.

For measurement of high-side V_{GS} (X20) and V_{DS} (X18), there are two footprints available that can be populated with connectors to attach isolated probes. Using these nodes is only recommended with optical isolated probes. If study of free-wheeling and reverse-recovery behavior is of interest, it is often sufficient to connect the test inductor between V_{SW} and PGND and to use the high-side input X2 for the double pulse test. In that way, relevant waveforms can all be captured safely through the low-side connectors X5-7.

CAUTION: There is high risk of shock and damage of the equipment if non-isolated probes are attached to X18 and X20.

5. Using the board for double-pulse testing

5.1. Required equipment

In order to perform double-pulse testing with this evaluation board, the following equipment is required:

- Isolated HV supply, I ≥ 0.2 A. **Note the maximum input voltage of the board is 450 VDC**.
- Isolated 12 V supply I ≥ 0.5 A for auxiliary circuit.
- Function generator with 50 Ω output impedance.
- Modern oscilloscope with high bandwidth (>500 MHz) and high sample rate (≥2 GS/s) together with:
  - HV passive probe for V_{DS} measurement
  - Passive probe for V_{GS} measurement, ideally with BNC adapter
  - High-quality (double-shielded) SMA to BNC coaxial cable for I_S measurement
  - Current probe for inductor current measurement (optional)

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5.2. Setup of measurement equipment

Careful preparation and setup are prerequisites for getting meaningful and repeatable double-pulse test results:

- **Probe compensation**: Automatic or manual probe compensation prior to starting the measurement is important to minimize offset and amplitude errors.
- **Removal of offsets**: Using passive probes at the low-side measurement nodes is recommended. If active probes are used instead, it is important to calibrate and auto-zero the probes prior to powering up the evaluation board.
- **Running at full bandwidth and high sample rate**: Please make sure that no reduced bandwidth settings are utilized for channels that are used for switching analysis and that high horizontal sample rate is chosen.
- **Using the full vertical scale**: Adjusting the vertical scale so the waveform will fill most of the screen without clipping will maximize resolution and helps to reduce noise.
- **Separating measurement and power cables**: Avoid routing measurement cables adjacent to power lines to reduce coupling, especially when measuring fast switching transitions.
- **Interpolation**: Use linear interpolation between samples. sin(x)/x is not suitable for accurate display of fast switching transitions.
- **De-skewing:** Compensating delay times of different probes is crucial for proper switching energy loss calculation and analysis of circuit behavior. Typical delay times can often be found in the data sheets of probes and coaxial cables but these values can deviate for the equipment in use by 100s of picoseconds. For highest precision, it is recommended to specifically de-skew the equipment used for the experiment. An easy to set up method that does not require a dedicated fixture is:
  1. First, measure the propagation delay of the coaxial cable for current measurement. Split a square wave voltage signal from the function generator by using a T-type BNC (male to 2x female) adapter. As shown in Fig. 11, connect the adapter directly to the 50 Ω input of channel A and route the same signal through the SMA/BNC coaxial cable under test to channel B. A small BNC to SMA adapter is required for the attachment and adds a delay of roughly 80 ps. By matching the edges of the waveforms in both channels, the de-skew value for the coaxial cable can now be determined. Using the averaging mode of the oscilloscope can facilitate finding a good match.
  2. Once the propagation delay of the coaxial cable is known, it can serve as reference for other probes and cables. By moving the T-type BNC adapter directly to the function generator output, the propagation delays of the remaining probes can be determined in the same manner, as illustrated in Fig. 12. In all cases, the propagation delay of the adapter should be subtracted as it will be removed before the double-pulse test.
     Note: Due to longer PCB traces, the propagation delay of the V_{DS} node on the evaluation board is approx. 200 ps higher than that for I_S. For maximum precision, this mismatch should be corrected as part of the de-skewing process.

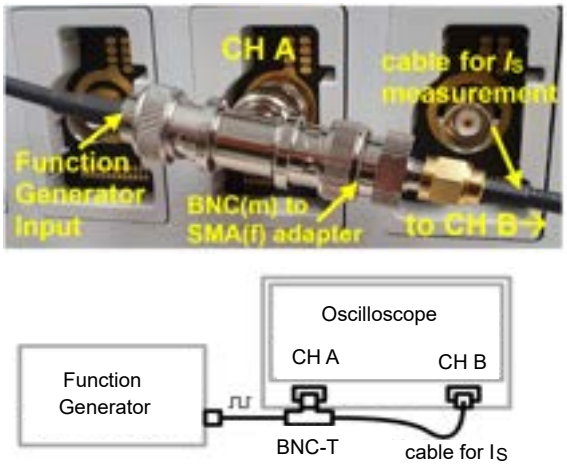


Fig. 11. Coaxial cable de-skewing setup



Fig. 12. Setup for measuring delay time of passive probes

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5.3. Start-up and shut-down sequence

Start-up:

1. Make sure all probes are properly compensated, de-skewed and additional settings (e.g. attenuation) are applied before connection to the board. Probes should be securely held in place with probe holders.
2. Set up all connections (AUX supply, HV supply, test inductor, probes) to the board prior to start up. Ensure that the jumpers X3 and X4 are in the correct position. For double pulse, independent pulse mode (right side position, Pin 1-2) is recommended.
3. Turn on the 12 V AUX supply. All three LEDs should light up.
4. Turn on the HV power supply and gradually increase voltage. For double-pulse testing, current limit as low as 0.1 A can be used. Maximum voltage is 450 V.
5. Send double pulse waveform to board via 50 Ω SMA input X1. Use of 3.3 V high-level is recommended.

Notes:

- When using the original inductor (approx. 18 µH), current ramp up at 400 V will be approx. 22 A/µs.
- Effective SMD shunt resistance will be close to 47.5 mΩ. It‘s best to compare against a precise external current sensor such as TCP0030A at initial setup to ensure all scope settings are accurate.
- For high current testing, adding external capacitance between X8 and X9 can help to stabilize the test voltage. Connection to the external capacitors must be low inductance.
- Double-pulse tests should only be performed in single-shot mode or with a sufficiently low repetition rate to prevent overheating.

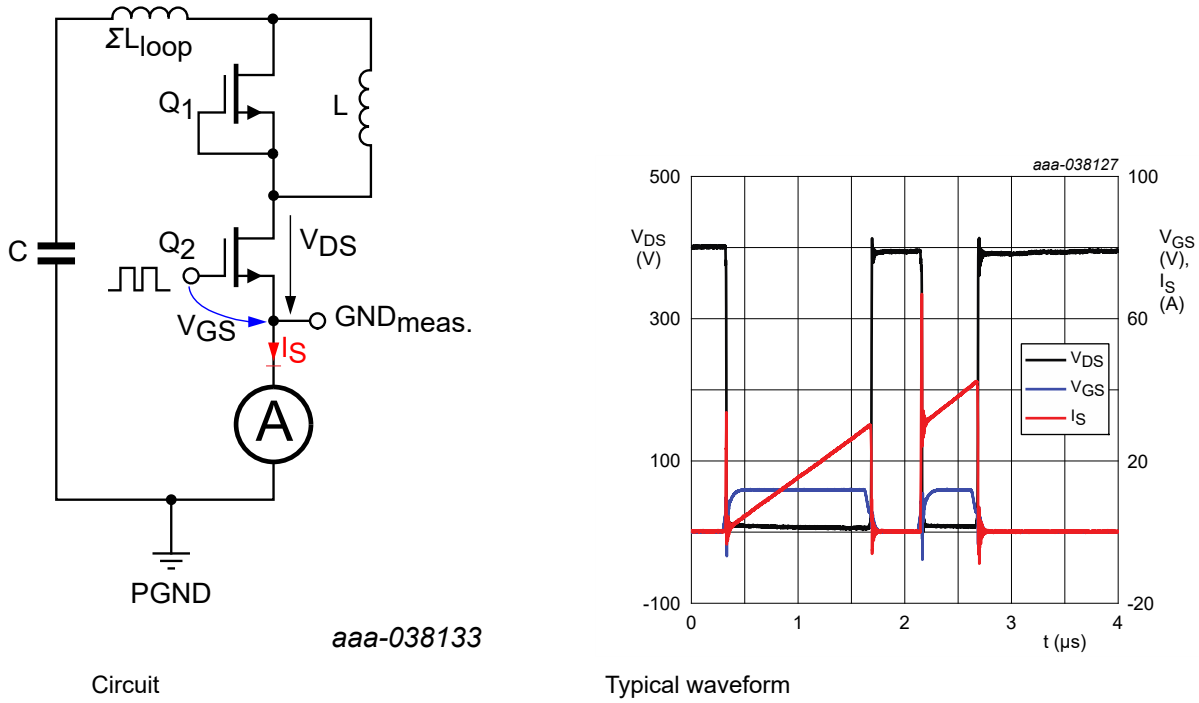
Shut-down:

1. Turn-off the HV power supply and wait for full discharge of the DC capacitors.
2. Turn-off the 12 V AUX supply.
3. Wait for full discharge before disconnecting the probes and power connections.

6. Double-pulse testing and typical results

When running the evaluation board in double-pulse mode (see Fig. 7) with the provided test inductor and unmodified gate circuitry, typical switching waveforms as shown in Fig. 13 can be measured at the low-side measurement nodes of the evaluation board. By variation of HV supply voltage and length of the first pulse sent by the function generator, turn-on and turn-off switching behavior at a wide range of currents and voltages can be investigated. All the measurements in this segment have been performed with a 1 GHz Tektronix MSO58 oscilloscope, 1 GHz TPP1000 passive probe with BNC adapter for V_{GS}, 800 MHz TPP0850 passive probe with common spring for V_{DS} and a 1 m non-magnetic double shielded Aircell 5 SMA to BNC coaxial cable for I_S.

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Circuit Typical waveform

Fig. 13. Circuit for double-pulse test and typical waveform for V_{DS} = 400 V, V_{GS} = 12 V, $I_{S,test}$ = 30 A

6.1. Evaluation of switching losses

Naturally, the first turn-on transition always occurs at 0 A. Once the gate of the low-side FET Q2 has been charged up beyond its threshold voltage, its channel starts to open. Current flow will increase and begin to discharge the device's output capacitance. This leads to the dissipation of E_{oss} in the channel but since the current loop is internal, it will not be measured by the external current sensor. However, the output capacitance of Q1 and any additional parasitic capacitance associated to the switch-node V_{SW} will be charged in the same interval. These currents flow through both Q2 and the current sensor and can be seen in i_S as a characteristic current peak during the transition. The total charge measured includes Q_{oss} of Q1 and the sum of charge on all parasitic capacitances C_{par} connected to vsw, such as winding capacitance of the test inductor, PCB layer capacitance, capacitance to the heat sink or gate driver supply capacitance.

Since this transfer of charge happens while V_{DS} is still relatively high, minimization of these parasitics is required for low switching losses and all parts of the evaluation board are optimized for very low capacitance. The waveforms of the first turn-on transition of the double pulse test at 200 V - 400 V are displayed in Fig. 14. Calculation of the instantaneous power loss $P_{sw} = V_{DS} \times I_S$, either directly on the oscilloscope or in an external tool enables evaluation of the minimum hard-switching turn-on loss E_{on} (0 A) through integration. Since the inductor current is very low, choosing the start and end for the loss integration is straightforward. Typically, the results should match fairly well with an estimated value of:

$$E_{on\,(0\,A)} \approx \left(Q_{OSS\,(V_{DC})} + 0.5 \times C_{par} \times V_{DC} \right) \times V_{DC} - E_{OSS} \quad (1)$$

At 400 V, E_{on}(0 A) in the range of 50 - 60 µJ is expected for GAN039.

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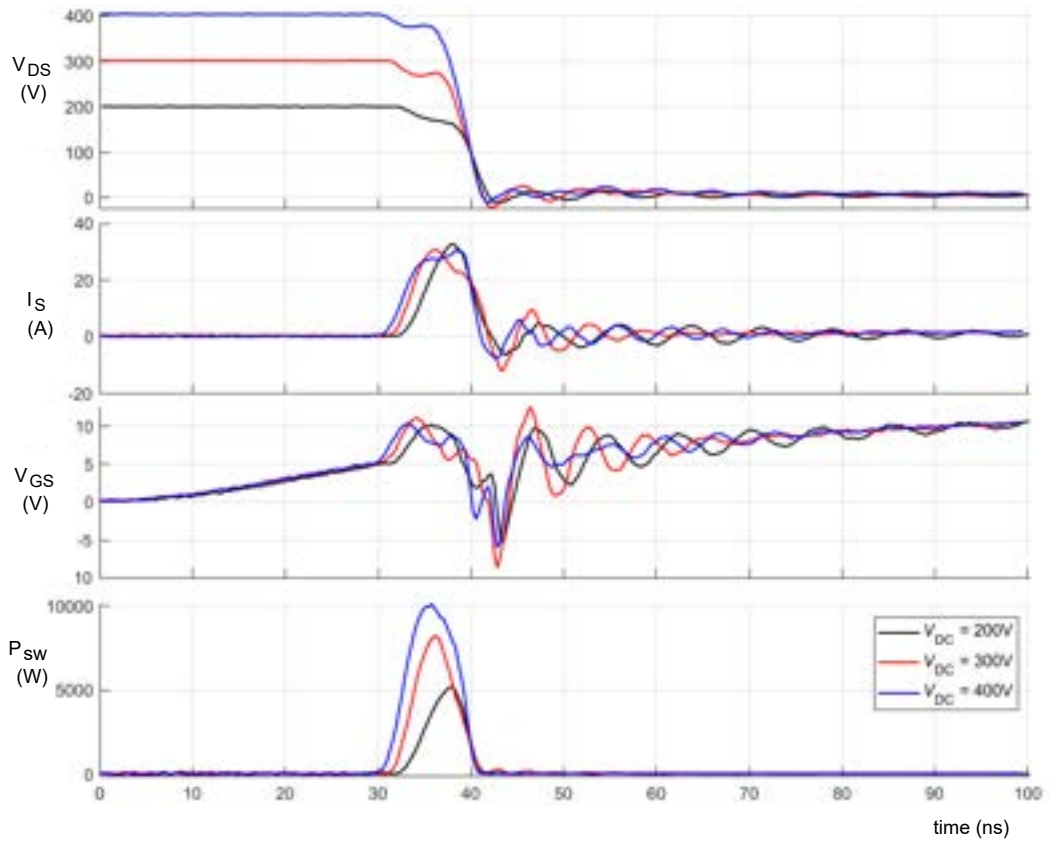


Fig. 14. Turn-on waveforms and instantaneous power loss P_{sw} at 0 A for V_{DC} = 200 V … 400 V

More interesting than the first turn-on transition are the following two switching transitions which occur at the same current levels, which can be set freely by variation of the first pulse length of the double pulse waveform. The waveforms in Fig. 15 depict the turn-on transitions of four individual test runs at inductor current levels from 10 A up to 40 A. For easier visibility, the curves are aligned at $V_{DS} = V_{DC}/2$. Clean transitions with very low ringing and consistent voltage slope of approx. -70 V/ns and current slopes of 5 - 6 A/ns can be seen. Although the devices do not use a Kelvin source connection, only small feedback on the gate occurs due to the low parasitic common-source inductance of the CCPAK. This feedback can be seen as shift of the V_{GS} waveforms when there is a high rate of change in the source current I_S.

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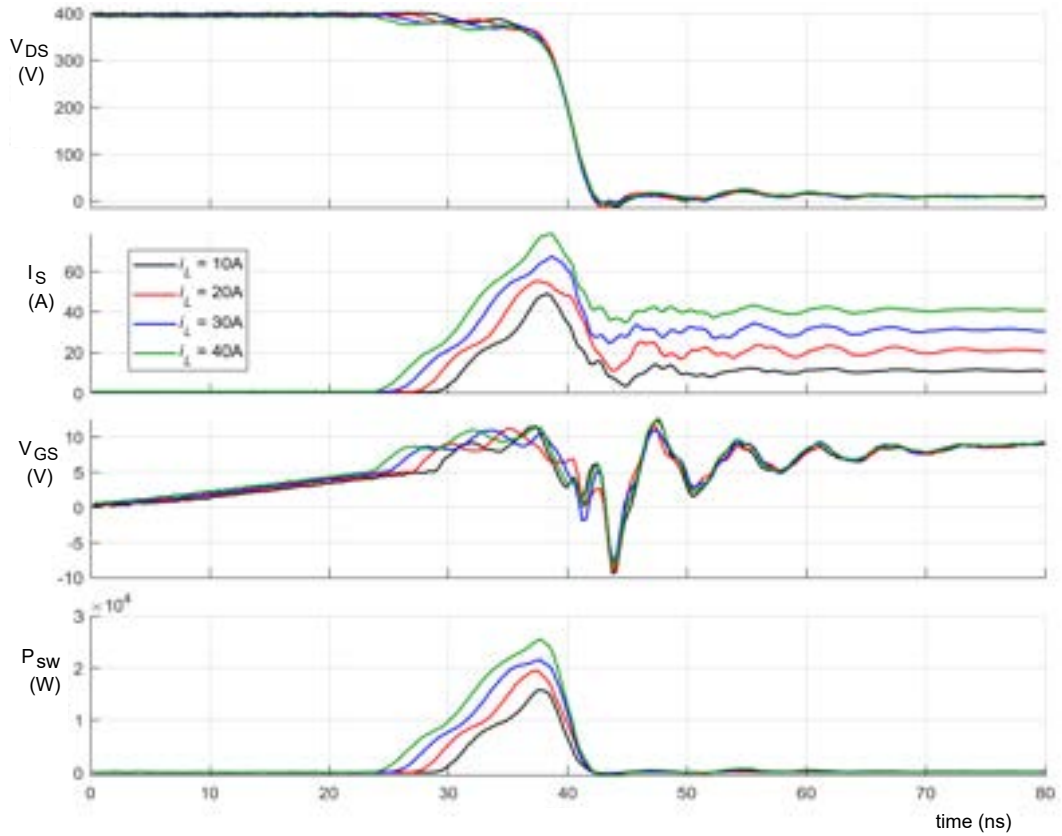


Fig. 15. Turn-on waveforms and instantaneous power loss P_{sw} for 10 A .. 40 A at V_{DC} = 400 V

Even though the switching slopes of GaN devices can be very fast and reverse recovery is only a minor effect, there is switching loss during hard switching, and the majority of that loss occurs during the turn-on transition. During the current slope, the voltage across the active FET is close to the DC supply voltage as long as the free-wheeling device still carries current and thus clamps the voltage. In a low inductance design, only a small dip on V_{DS} due to the voltage drop across the total loop inductance $\sum L_{loop}$ will occur. Therefore, peak values of P_{sw} are significant in size and it is again relatively easy to find the start and stop intervals for the switching energy integration. Nevertheless, it is recommended to not overly extend the upper limit of the interval when running at high current levels to not falsely add conduction losses into the calculation.

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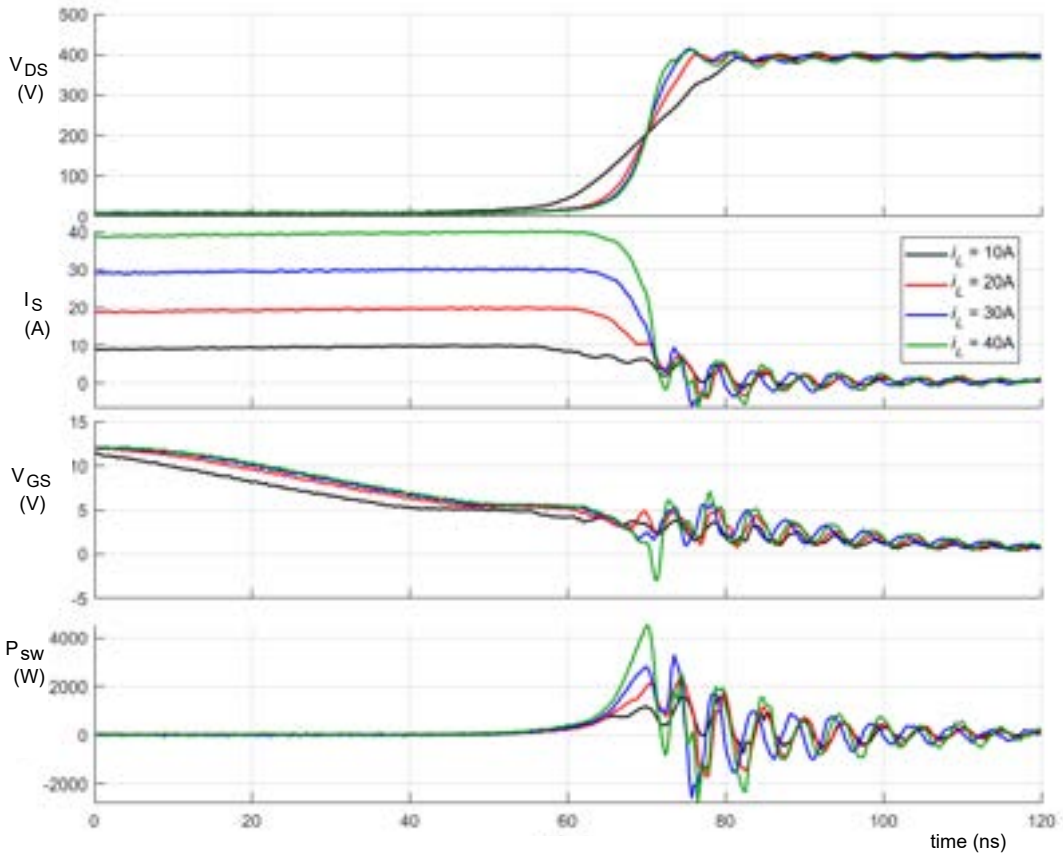


Fig. 16. Turn-off waveforms and instantaneous power loss P_{sw} for 10 A .. 40 A at V_{DC} = 400 V

In contrast to turn-on, the turn-off transitions as shown in Fig. 16 are strongly affected by the level of load current. Even at a moderate gate resistor of 15 Ω, GAN039 is able to pinch-off the channel very quickly and the majority of the load current will charge up the output capacitance of the FET instead of being dissipated in the channel. This leads to a load dependency of the voltage- and current slopes. Again, the waveforms on the evaluation board look clean with little overshoot and only very moderate amount of ringing. Precise extraction of the turn-off losses in double-pulse is challenging for fast GaN devices. Simply integrating P_{sw} will capture not only the dissipated losses in the channel but also the nearly lossless storage of energy E_{oss} onto the parasitic capacitance of the device. Unless the GaN FET is slowed down significantly, E_{oss} can be several times larger than the dissipated power. The typical ringing of output capacitance with commutation inductance after turn-off adds to the challenge as the integration period might have to be lengthened in order to ensure that the evaluation is stopped only when the steady-state voltage is reached. Otherwise, the differences in energy storage might be wrongly attributed to switching losses. The need for a longer integration period also leads to challenges regarding offsets. While these can usually be compensated in post-processing, it might be tricky to do so when running the analysis directly on the oscilloscope.

With that being said, the requirement for strictly splitting dissipative loss components from the capacitive energy E_{oss} is only especially crucial when designing for soft-switching applications. In these, E_{oss} can be recovered during nearly lossless zero-voltage turn-on and the small amount energy dissipated at turn-off will form the main part of the total switching loss. The precision of the standard double-pulse test is limited in this case and alternative ways to evaluate, such as calorimetric testing, can lead to better results.

When estimating total losses in hard-switching applications, splitting of the total turn-off energy is usually not required, as E_{oss} will be dissipated internally in the following turn-on period. Therefore, simply adding directly measured E_{on} and E_{off} will lead to good results.

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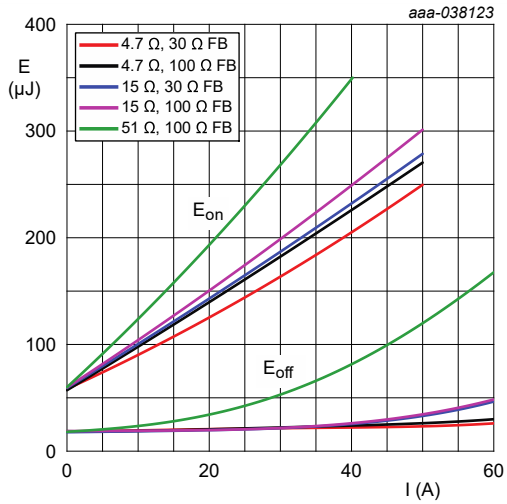


Fig. 17. Switching losses of GAN039 at V_{DC} = 400 V for different gate configurations at room temperature

An overview over switching energies at V_{DC} = 400 V and room temperature is depicted in Fig. 17 The standard configuration using gate resistors R_G = 15 Ω in series to a 30 Ω (@100 MHz) ferrite bead is shown in blue. The graphs confirm very low switching energies even at moderate gate resistor values, especially for turn-off.

6.2. Switch timings, voltage slopes and inductance extraction

Additional information can be extracted from the switching waveforms and some of the parameters for turn-on can differ considerably between different test circuits for one single device. This is due to the voltage dip introduced by the commutation loop inductance at turn-on and due to the popular way of using 90% of the steady-state voltage level as a reference for some evaluations, such as the switch timings shown in Fig. 18 or voltage slopes. Under the assumption of uniform current change in the commutation loop, the voltage dip can be calculated as:

$$v_{DS,dip} = -\Sigma L_{loop} \times di_S/dt \quad (2)$$

If the platform does not have sufficiently low inductance or the current slope is very high, $V_{DS,dip}$, might lead to V_{DS} dropping below 0.9 × V_{DC} early.

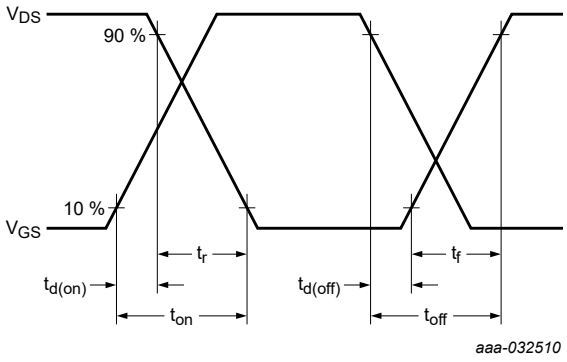


Fig. 18. Typical switching time waveform

Fig. 19 shows an exemplary turn-on waveform at 400 V and 30 A on the evaluation platform and it can be seen that V_{DS} starts to drop below 0.9 × V_{DC} only after the measured current peak exceeds the turn-on current significantly. Therefore, no early dip has occurred and the extracted timings will be accurate, which is important for example when trying to optimize the dead-time. In the present case, the markers indicate a turn-on delay time $t_{d(on)}$ ≈ 31.4 ns, t_r ≈ 4.5 ns and dV/dt of -71 V/ns.

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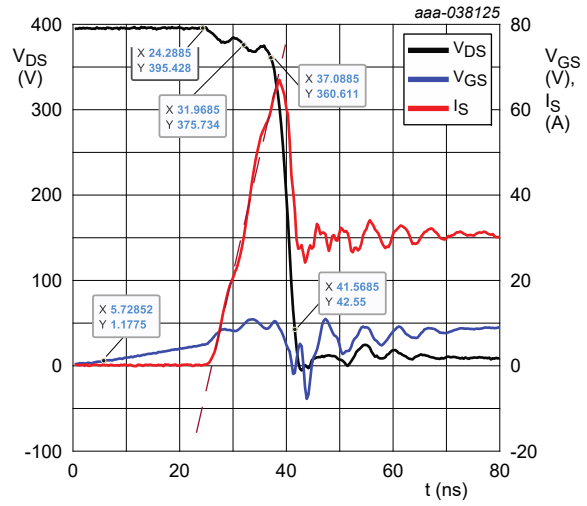


Fig. 19. Turn-on waveform at 400 V and 30 A with characteristic markers for switch timing and inductance extraction

The voltage dip can also be used to estimate the commutation inductance of the board, which is one of the main performance parameters of any design and should generally be minimized for best switching performance. Using the information from Fig. 19, the estimated inductance of the commutation loop of the evaluation platform including DC-link capacitors, PCB, current sensor and two GAN039 FETs in CCPAK can be calculated as:

$$\Sigma L_{loop} \approx \frac{v_{DS,dip}}{\left(di_S/dt\right)} = \frac{20\ V}{5.4A/ns} = 3.7\ nH \tag{3}$$

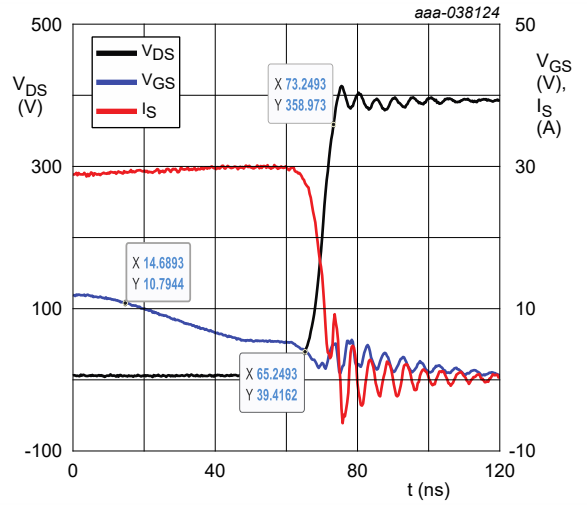


Fig. 20. Turn-off waveform at 400 V and 30 A with characteristic markers for switch timing

In a similar manner, the timings for turn-off can be extracted, as demonstrated in Fig. 20 with a turn-off delay time $t_{d(off)} \approx 50.6$ ns and $t_f \approx 8$ ns. At turn-off, the layout has no strong impact on the readings and numbers should be comparable between different platforms. Again, extraction of parasitic inductance can be performed using the frequency f_r of the ringing on V_{DS} and I_S after turn-off. It is recommended to pick several periods in a segment that is close to the steady state voltage to improve reading precision for f_r.

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From Fig. 19, a frequency f_r = 198 MHz at approx. 392 V can be seen. In combination with an estimated total parasitic capacitance for the PCB, test inductor, heat sink etc. of 40 pF, the total commutation loop inductance is calculated as:

$$\Sigma L_{loop} = \frac{1}{\left[(2\pi f_r)^2 \times (C_{oss} + C_{par})\right]} \approx \frac{1}{\left[(2\pi \times 198MHz)^2 \times (150pF + 40pF)\right]} \approx 3.4\ nH \quad (4)$$

which is fairly close to the results from the v_{dip} method.

Note: Sometimes, the switch timings are used for switching loss estimations based on a triangular approximation of the transitions. This approach can be fairly accurate for fast turn-off transitions (including E_{oss}) but they will not be able to reliably predict the significantly larger turn-on energy without using more sophisticated math. In addition, unexpected effects such as parasitic turn-on or excessive reverse-recovery might not be represented by the data available. Therefore, measurement of the switching transitions is always the recommended approach.

6.3. Performance in third quadrant

One of the key benefits of GaN HEMTs is the absence of stored minority carries when conducting in reverse direction due to the lack of a bipolar body diode. Instead, the device will turn its unipolar channel automatically on as soon as sufficient reverse voltage is applied. While e-mode FETs can have significant forward voltage drop V_F during this conduction phase, especially when turned-off with a negative gate voltage, the Si-FET in the Cascode will always ensure low V_F. Nevertheless, synchronous rectification, thus actively turning on the device through the gate in third quadrant, can help to further improve efficiency.

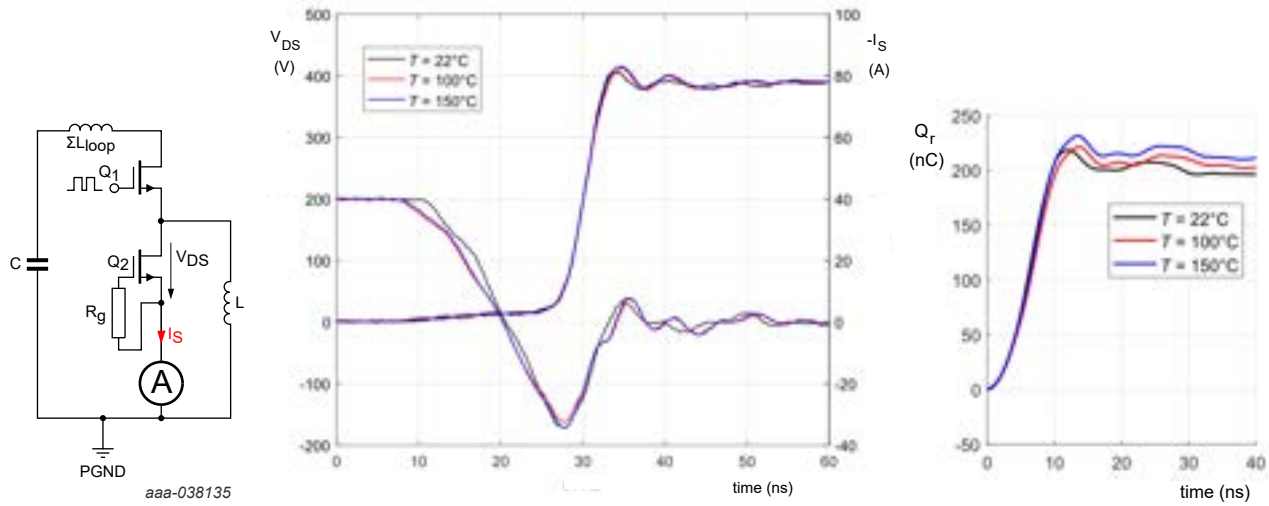
Since the body-diode of the Si-FET in the Cascode is used for third-quadrant conduction, the device will show an increase in total charge beyond Q_{oss} due to diffusion of minority carriers Q_D. However, the Si-FET is a low-voltage device and its injected charge is orders of magnitude smaller than that of high voltage Si-superjunction FETs. It is also much smaller than the static Q_{oss} of the cascode for all operating conditions. The total recovered charge in reverse-recovery after hard turn-off is given as:

$$Q_r = Q_{OSS} + Q_D \quad (5)$$

Double-pulse evaluation of reverse-recovery can give vital insights on how the device will perform under application-typical conditions as data sheet information is often limited. Parameters such as device temperature, switched current level or current slope can have a strong impact on the magnitude of the injected charge in Si- and SiC MOSFETs and snappy turn-off behavior might lead to problems with stability and EMI. Since Q_D is low, this is not an issue for GAN039 and there is only a minor sensitivity to changes in temperature, switched current and current slope.

To measure Q_r, the test inductor must be connected from switch-node to power GND and the gate trigger signal should be sent to the high-side FET Q1 instead, as shown in Fig. 21 a). Using the low-side measurement nodes, typical waveforms as shown in Fig. 21 b) can be captured and integrating the measured current from zero-crossing until the steady-state voltage results in Q_r. Integrating until voltage steady-state and after decay of current ringing is important to get repeatable results and in case of longer integration periods, compensation of current offset might be necessary. This works most reliably in post-processing. Fig. 21 c) shows the Q_r results for different device temperatures for a measurement at 400 V and 40 A in Fig. 21 b). Only a small increase of Q_r of roughly 15 nC due to the increase in temperature from room temperature to 150 °C is measured in this example. It should be noted that V_{DC} is not entirely constant due to the high current level. This will not impact the results significantly but if voltage stability is a concern, a low inductance capacitor can be added to the input nodes of the board.

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a) test configuration

b) typical switching waveforms different temperatures

c) integrated charge after zero-crossing of I_S

Fig. 21. Reverse-recovery test configuration and waveforms; V_{DC} = 400 V ; I_{load} = 40 A

6.4. Performing measurements at elevated temperature

Power semiconductors are rarely operated at room temperature and double pulse evaluation at higher temperature can give helpful information for the design of the heat sink. The GAN039 evaluation board comes pre-equipped with a pin fin heatsink and while specific temperatures can be achieved with smart operation in this setup, it is much more convenient to replace the heat sink with an external heat source. Attaching a similarly sized plate of aluminum with a high-temperature heating resistor is a simple and effective solution. Since GAN039-650NTB is a top-side cooled device, the temperature being set at the Al-plate is very close to the junction temperature T_j but it is always best to confirm temperatures during use by means of an IR camera. For that, there are two holes in the PCB located directly above the hot spot of the devices that can be used for temperature measurement. Since the devices are heated externally, the readings on the top side of the PCB are only slightly lower than the internal junction temperature of the devices. Fig. 22 illustrates the heating plate setup and an IR measurement at $T_j \approx 150$ °C.

Note: When changing the heatsink, please always check for proper insulation before applying the supply voltages and make sure that all components and cables can sustain high temperatures.

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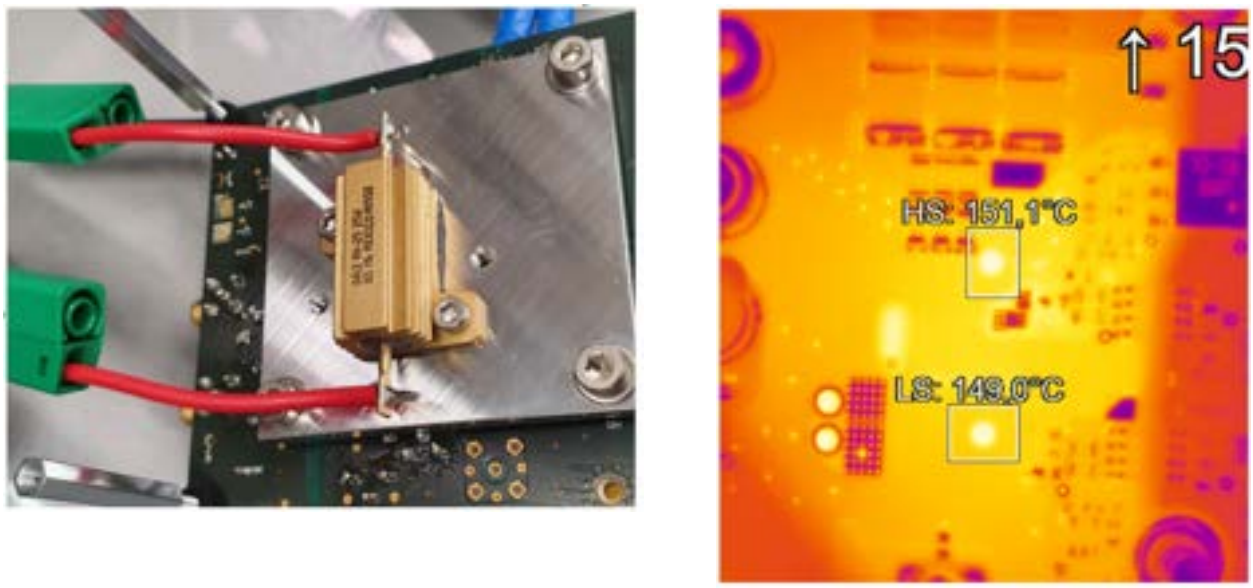


Fig. 22. Test setup for double pulse at elevated temperature (bot) and temperature reading from the top-side using an IR camera

GAN039 is a fast GaN Cascode device with very good switching performance even at high temperature. The two most relevant temperature-sensitive parameters from an application point of view are the threshold voltage V_{th} and the transconductance of the device. Both will decrease when temperature rises, leading to a small change in switch timings and turn-on di/dt. Exemplary turn-on waveforms as well as the switching energy losses at different temperatures are depicted in Fig. 23.

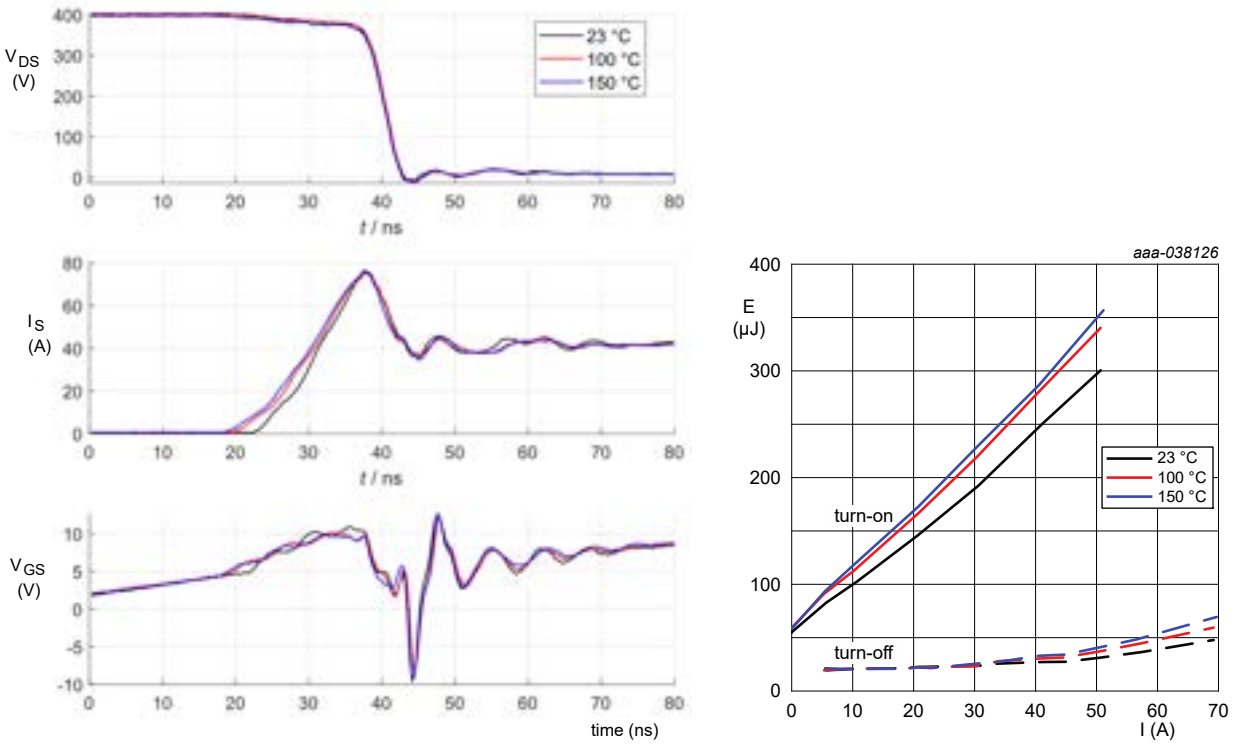


Fig. 23. Temperature variation impact on turn-on waveform and switching energy losses

The slight decrease in switching slope is the main reason for the increase in turn-on loss as Q_r remains nearly constant, as demonstrated in the previous section. The turn-off losses only start to noticeably change beyond 30 A and this level can be shifted upwards by using a lower gate

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resistor if continuous high peak current operation is required. Due to the beneficial Q_{GD}/Q_{GS} ratio of GAN039, single gate supply voltage is sufficient when operating at maximum temperature and high switching speed.

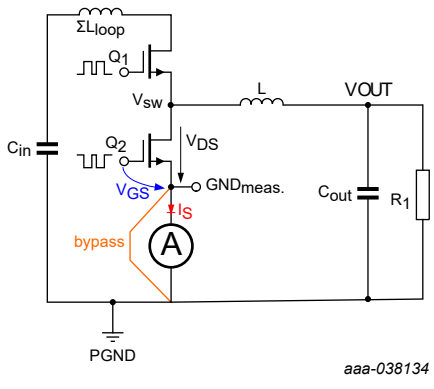
7. Continuous operation

7.1. Required modifications and limitations

To run the evaluation board in continuous operation, the equipment listed in Section 4.3 is required. When changing from double pulse testing, a few crucial changes and checks are required on the board as well:

1. **Bypass of the current sensor** (see Fig. 24) This is mandatory to not damage the sensor when running at high current level. Using standard solder for bypassing is sufficient but adding some copper wire or braid helps bridging the gap
2. Replacing the double-pulse test inductor with a larger inductor suitable for continuous operation. Connect this inductor between V_{sw} and V_{out}.
3. Setting the gate signal selectors (X3, X4) to either use both gate signal inputs or a single input plus fixed on-board dead time generation. Always make sure there is sufficient dead-time prior to powering up.
4. Attaching a sufficiently rated load resistor or electronic load at the output pins X13 and X14
5. When running efficiency measurements, please make sure to attach the voltage sense cables directly at the power terminals of the board.

The main limitation of the board when running hard-switching tests at high switching frequency is usually the maximum junction temperature of the GaN FETs. It is generally advised to monitor the temperatures of the board using an IR camera during challenging test runs. The PCB consists of four 70 µm copper thickness layers and the half-bridge is designed to handle a minimum of 30 A DC current at room temperature. When running in extreme conditions such as very high ripple triangular current, please make sure to check that the ripple current rating of the capacitors on the board is sufficient.



test configuration



current sensor is bypassed on the top-side using a braid wire solder bridge

Fig. 24. Modified double pulse evaluation board for buck converter operation

7.2. Example 100 kHz buck converter test

This section presents typical test results for an efficiency sweep in buck converter operation with the evaluation board. The board is operated at V_{in} = 400 V and V_{out} = 230 V with the standard fixed on-board dead-time (approx 80 ns) and a switching frequency of 100 kHz, which is a good choice for high efficiency operation at moderate inductor size. The test inductor is shown in Fig. 24 and consists of an MPP toroid C055439A2 with 50 turns of solid wire and has a no-load inductance of approx. 330 µH. For efficiency measurement, a Yokogawa WT5000 power analyzer is used and its voltage sense connections are attached directly to the input and output power connectors of the board (not shown in Fig. 24). The efficiency curve of this test under normal laboratory conditions is depicted in Fig. 25. High hard-switching efficiency exceeding 99% across a wide power range

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and a peak above 99.1% can be observed. The reduction in efficiency when also including the auxiliary power losses is mainly due to the power draw of the 12 V fan. The test board is capable of exceeding 5 kW in this test but the pin-fin heat sink will slowly heat up if no additional source of air flow is used. On a cold plate with fixed water temperature, output power exceeding 7 kW can be achieved in combination with a suitable inductor.

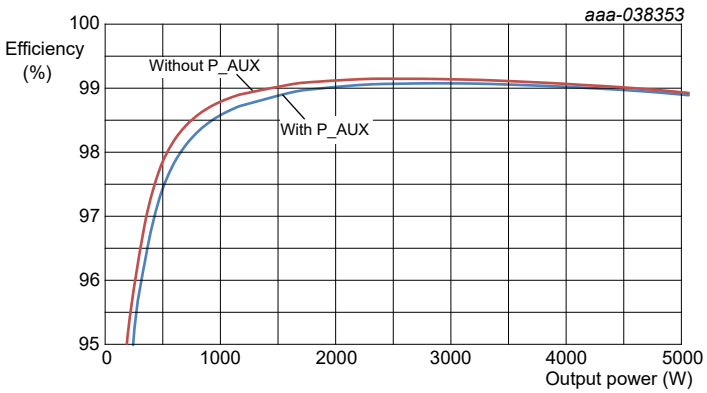


Fig. 25. 400 V to 230 V conversion efficiency in buck converter mode at 100 kHz using pin-fin heat sink

8. Thermal stack investigation

One of the great advantages of top-side cooled packages is the low total thermal resistance as only an insulating thermal interface material is required between the device and the heat sink. In comparison with conventional SMD devices that require heat extraction on the bottom side through the PCB, thermal resistance of a good setup can be reduced from 4-6 K/W to easily below 2 K/W with top-side cooling. This helps optimizing efficiency, power density or reliability of the components significantly.

Especially for high power converters, it is important to assess the thermal resistance of the chosen thermal stack to prevent overheating. A simple way to evaluate temperature rise versus device loss is a DC current test. For this test, both power semiconductors are turned on at the same time and a high current source is used to push constant current through the devices. Since only conduction losses occur, calculation of the individual power dissipation per FET only requires measurement of the supply current and the individual device voltages. By measuring the surface temperature using an IR cam, an estimation of the thermal stack performance can be made.

In order to turn both devices on at the same time, the overlap protection described in section 4 has to be defeated by soldering resistors R41 and R42 to their adjacent pads, as shown in Fig. 26. **This modification must only be used for thermal tests at very low supply voltage and needs to be reverted to the original state before doing any test at higher voltage to prevent damage to the board.**

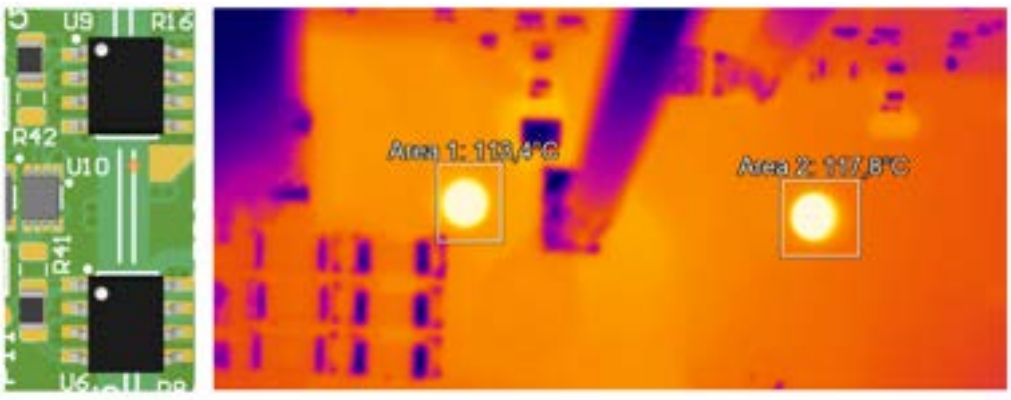


Fig. 26. Modification of R41, R42 to defeat overlap protection for R_{th} testing (left) and thermal image of the device surface temperatures through PCB holes (right)

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The thermal resistance estimation relies on accurate measurement of the surface temperature and the device losses. It should be noted that the internal junction temperature will be slightly higher than the reading of the IR camera at the surface, especially when high power (>50 W) is drawn from each FET. Nevertheless, since the main thermal path is on the opposite side of the device, the reading gives a fair approximation of $T_c \approx T_j$ and $R_{th(j-a)} = (T_j - T_a) / (V_{DS} \times I_{DC})$. The evaluation board comes equipped with a pin-fin heatsink. A 0.5 mm AlN shim and thermal grease are used to ensure insulation and good thermal interfacing. The total thermal resistance $R_{th(j-a)}$ from junction to ambient is in the range of 3 K/W. The main limitation is the limited power dissipation capability of the small heat sink and by moving the same setup onto a cold plate, $R_{th(j-a)} < 1.5$ K/W can easily be achieved.

9. Design details

The NX-DP-GAN039-TSC CCPAK double pulse evaluation board schematic is shown in Fig. 27, and Fig. 28.

The NX-DP-GAN039-TSC CCPAK double pulse evaluation board PCB has 4 layers, these shown in Fig. 29, Fig. 30, Fig. 31 and Fig. 32.

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9.1. Schematics

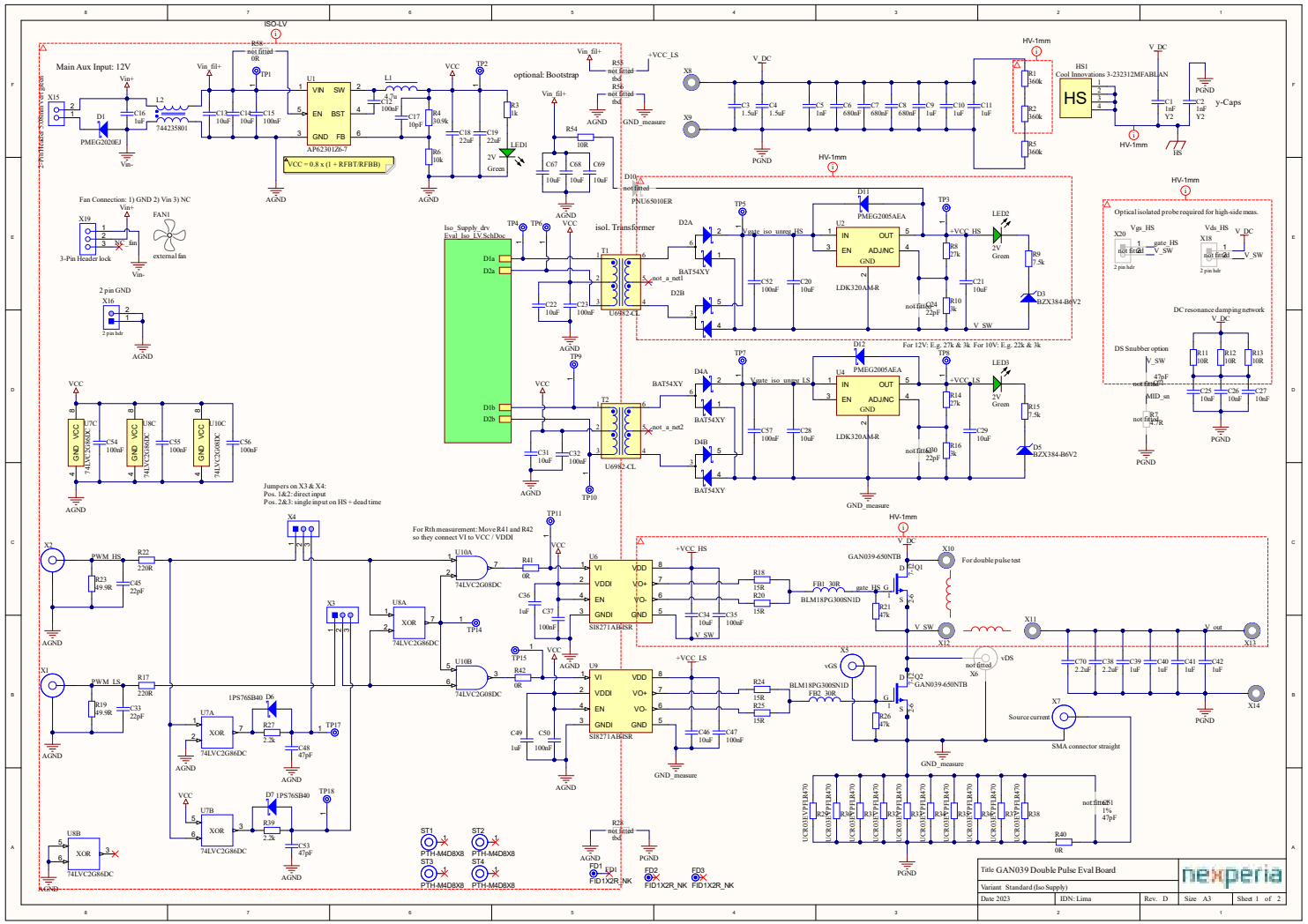


Fig. 27. NX-DP-GAN039-TSC CCPAK double pulse evaluation board schematic main sheet

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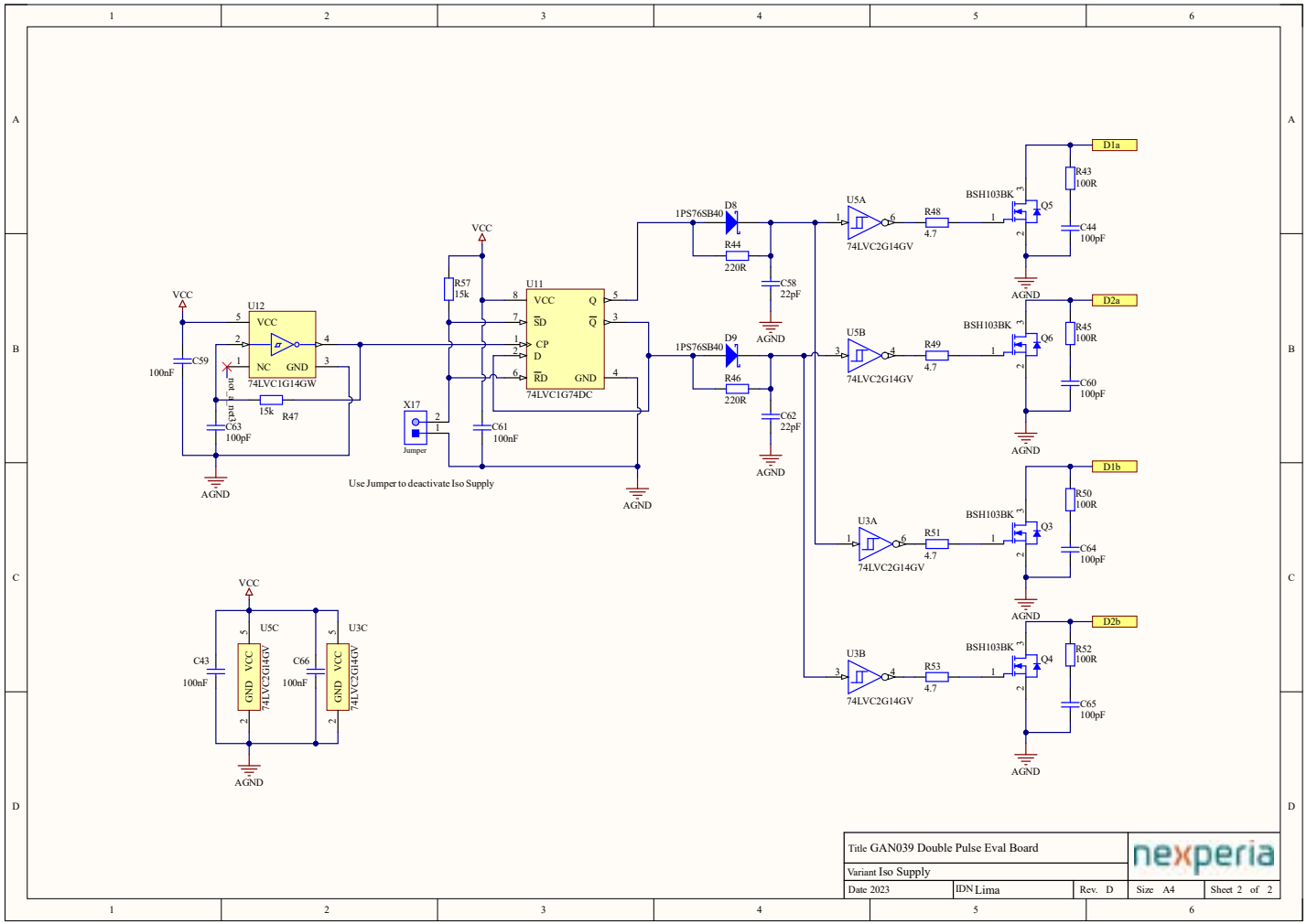


Fig. 28. NX-DP-GAN039-TSC CCPAK double pulse evaluation board schematic isolated supply sub-sheet

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9.2. PCB layout

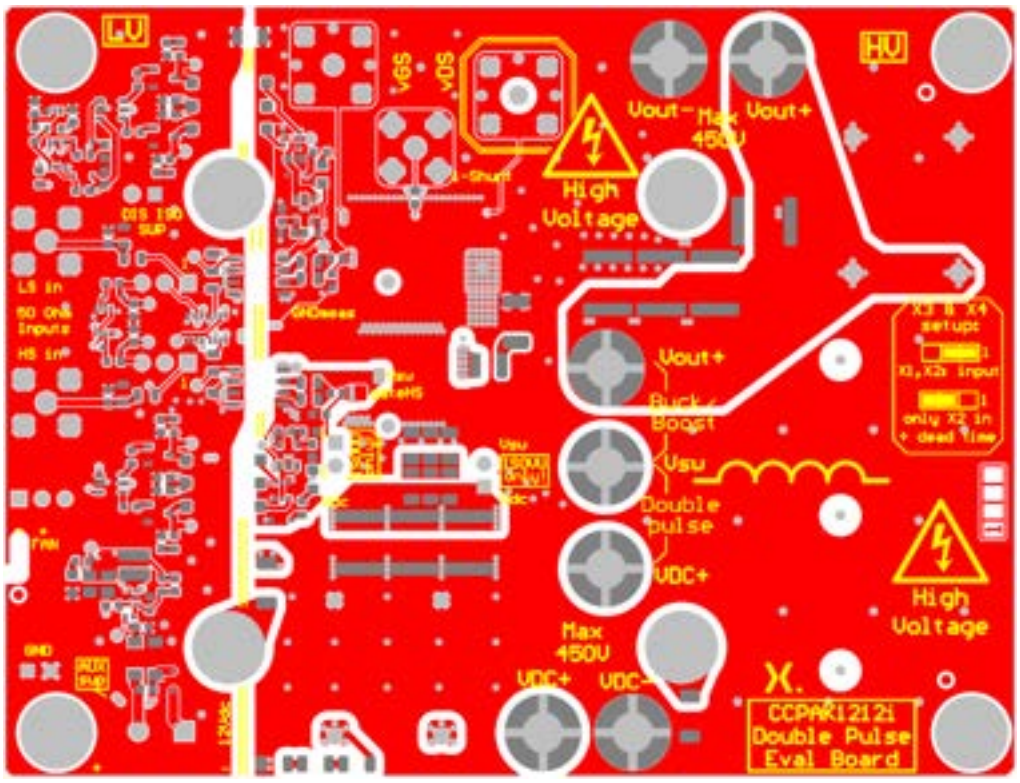


Fig. 29. NX-DP-GAN039-TSC CCPAK double pulse evaluation board PCB top layer

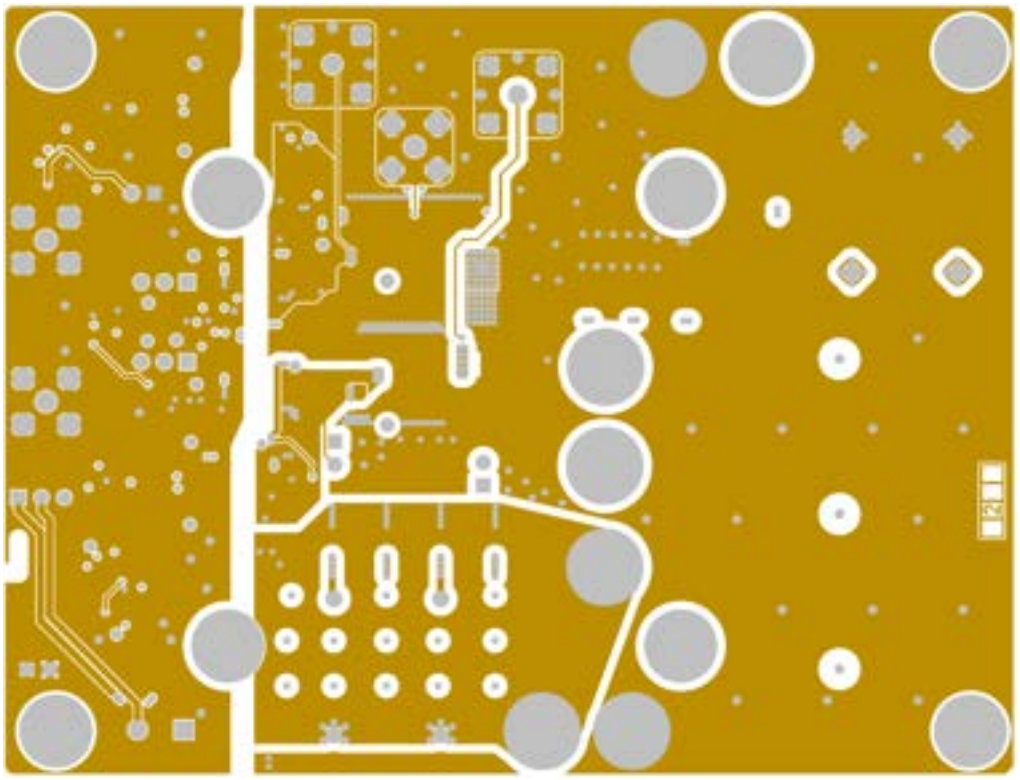


Fig. 30. NX-DP-GAN039-TSC CCPAK double pulse evaluation board PCB inner layer 1

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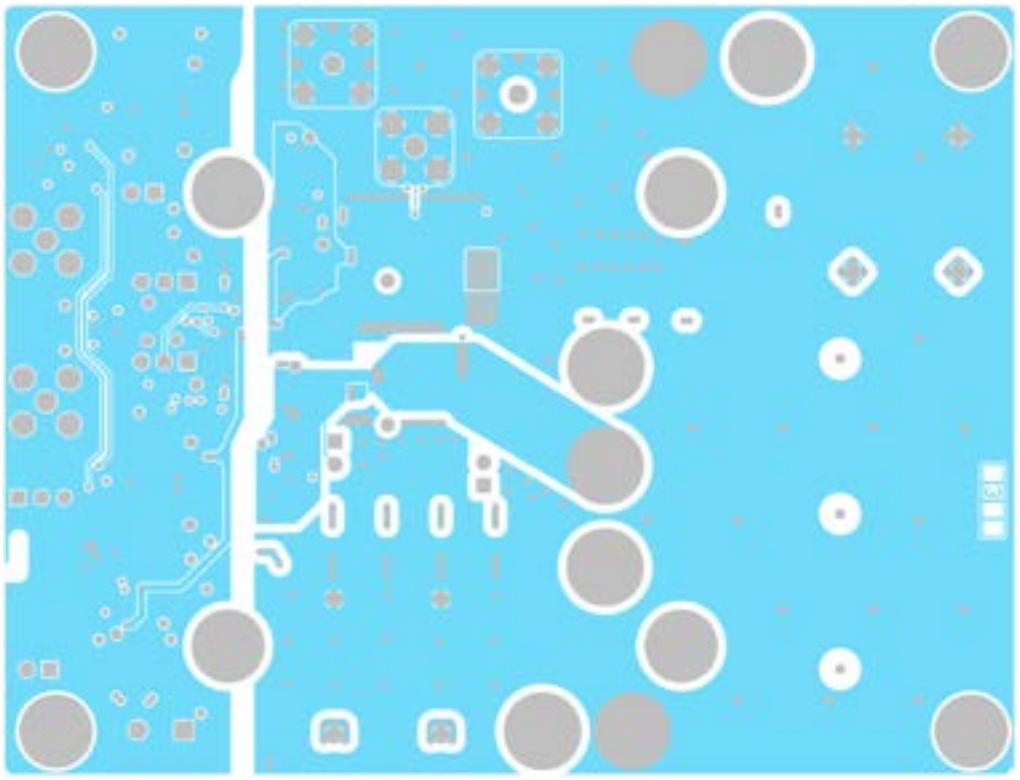


Fig. 31. NX-DP-GAN039-TSC CCPAK double pulse evaluation board PCB inner layer 2

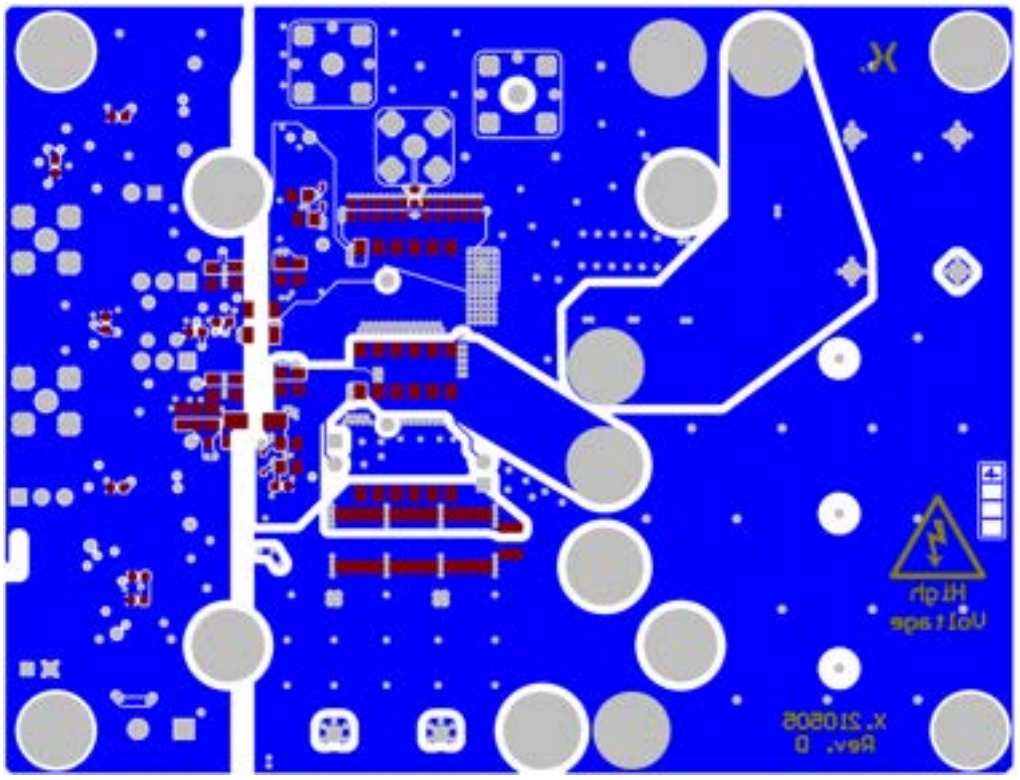


Fig. 32. NX-DP-GAN039-TSC CCPAK double pulse evaluation board PCB bottom layer

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9.3. NX-DP-GAN039-TSC CCPAK double pulse evaluation board Bill of Materials

Table 2. Bill of Material

Value	Description	Designator	Quantity	Manufacturer	Supplier P/N
CAP CER SAFETY Y2 1nF ±10% 250V X7R 1808	Safety Ceramic Capacitor Class Y2 1nF ±10% 250V X7R 1808	C1, C2	2	Murata	GA342DR7GF102KW02L
B32672P5155J003	Film Capacitor MKP 1.5uF ±5% 520V Radial shorter leads	C3, C4	2	KEMET	R71VI415050H6K
CAP CER 1nF ±10% 2kV X7R 1210	Ceramic Capacitor 1nF ±10% 2kV X7R 1210	C5	1	Yageo	CC1210KKX7RDBB102
CAP CER 680nF ±20% 450V X7T 2220	Ceramic Capacitor 680nF ±20% 450V X7T 2220	C6, C7, C8	3	TDK	CGA9M4X7T2W684M200KA
CAP CER 1uF ±20% 450V X7T 2220	Ceramic Capacitor 1uF ±20% 450V X7T 2220	C9, C10, C11, C39, C40, C41, C42	7	TDK	CGA9P4X7T2W105M250KE
CAP CER 100nF ±20% 25V X7R 0603	Ceramic Capacitor 100nF ±20% 25V X7R 0603	C12, C15, C23, C32, C43, C54, C55, C56, C59, C61, C66	11	KEMET	C0603C104M3RACTU
CAP CER 10uF ±20% 25V X5R 0603	Ceramic Capacitor 10uF ±20% 25V X5R 0603	C13, C14, C22, C31	4	TDK	C1608X5R1E106M080AC
CAP CER 1uF ±10% 25V X7R 0603	Ceramic Capacitor 1uF ±10% 25V X7R 0603	C16	1	Samsung	CL10B105KA8NNNC
CAP CER 10pF ±10% 50V C0G/NP0 0603	Ceramic Capacitor 10pF ±10% 50V COG/NP0 0603	C17	1	KEMET	C0603C100K5GACTU
CAP CER 22uF ±20% 25V X5R 0805	Ceramic Capacitor 22uF ±20% 25V X5R 0805	C18, C19	2	Murata	GRM21BR61E226ME44L
CAP CER 10uF ±10% 25V X7S 0805	Ceramic Capacitor 10uF ±10% 25V X7S 0805	C20, C21, C28, C29, C34, C46, C67, C68, C69	9	Murata	GRM21BC71E106KE11L
CAP CER 10nF ±10% 1kV X7R 1206	Ceramic Capacitor 10nF ±10% 1kV X7R 1206	C25, C26, C27	3	Wurth Electronics	885342208021
CAP CER 22pF ±5% 100V C0G 0603	Ceramic Capacitor 22pF ±5% 100V C0G 0603	C33, C45, C58, C62	4	KEMET	C0603C220J1GACTU
CAP CER 100nF ±10% 100V X7R 0805	Ceramic Capacitor 100nF ±10% 100V X7R 0805	C35, C37, C47, C50	4	KEMET	C0805X104K1RACAUTO

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Value	Description	Designator	Quantity	Manufacturer	Supplier P/N
CAP CER 1uF ±10% 50V X7R 0805	Ceramic Capacitor 1uF ±10% 50V X7R 0805	C36, C49	2	TDK	CGA4J3X7R1H105K125AB
B32672P4225K000	Film Capacitor MKP 2.2uF ±5% 450V Radial	C38, C70	2	TDK EPCOS	B32672P4225K000
CAP CER 100pF ±5% 100V C0G 0603	Ceramic Capacitor 100pF ±5% 100V C0G 0603	C44, C60, C63, C64, C65	5	Kyocera AVX	06031A101FAT2A
CAP CER 47pF ±1% 100V C0G 0603	Ceramic Capacitor 47pF ±1% 100V C0G 0603	C48, C53	2	KEMET	C0603C470J1GACTU
CAP CER 100nF ±20% 50V X7R 0603	Ceramic Capacitor 100nF ±20% 50V X7R 0603	C52, C57	2	Murata	GCJ188R71H104KA12D
PMEG2020EJ	Schottky Diode 20V 2A SOD-323	D1	1	Nexperia	PMEG2020EJ,115
BAT54XY	Schottky Diode Quadruple 30V 0.2A SOT-363	D2, D4	2	Nexperia	BAT54XY,115
BZX384-B6V2	Zener Diode 6.2V SOD-323	D3, D5	2	Nexperia	BZX384-B6V2,115
1PS76SB40	Schottky Diode 40V 0.12A Low Cap SOD-323	D6, D7, D8, D9	4	Nexperia	1PS76SB40,115
PMEG2005AEA	Schottky Diode 20V 0.5A SOD-323	D11, D12	2	Nexperia	PMEG2005AEA,115
BLM18PG300SN1D	Ferrite Bead 30Ohm 1A 0603	FB1, FB2	2	Murata	BLM18PG300SN1D
78438336047	Inductor 4.7uH ±20% 3.9A Isat 1.9A Irms 137mR	L1	1	Wurth Electronics	78438336047
WE-744235801	Common Mode Line Filter 1.3uH 1A 2LN 800 OHM SMD	L2	1	Wurth Electronics	744235801
150080VS75000	LED Green 2V 20mA 0805	LED1, LED2, LED3	3	Wurth Electronics	150080VS75000
GAN039-650NTB(A)	GaN FET 650V 33 mOhm CCPAK1212i (SOT8005)	Q1, Q2	2	Nexperia	GAN039-650NTB(A)
BSH103BK	MOSFET N-CH 30V 0.85A 3-Pin SOT-23	Q3, Q4, Q5, Q6	4	Nexperia	BSH103BKR
RES SMD 360k 1% 0.25W 1206	Chip Resistor 360k ±1% 0.25W 1206	R1, R2, R5	3	TT Welwyn	WCR1206-360KFI
RES SMD 1k 1% 0.1W 0603	Chip Resistor 1k ±1% 0.1W 0603	R3	1	Yageo	RT0603BRD071KL
RES SMD 30.9k 1% 0.1W 0603	Chip Resistor 30.9k ±1% 0.1W 0603	R4	1	Yageo	RC0603FR-0730K9L

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Value	Description	Designator	Quantity	Manufacturer	Supplier P/N
RES SMD 10k 1% 0.1W 0603	Chip Resistor 10k ±1% 0.1W 0603	R6	1	Yageo	RT0603BRE0710KL
RES SMD 27k 1% 0.1W 0603	Chip Resistor 27k ±1% 0.1W 0603	R8, R14	2	Vishay	CRCW060327K0FKEA
RES SMD 7.5k 1% 0.1W 0603	Chip Resistor 7.5k ±1% 0.1W 0603	R9, R15	2	Yageo	RT0603BRD077K5L
RES SMD 3k 1% 0.1W 0603	Chip Resistor 3k ±1% 0.1W 0603	R10, R16	2	Yageo	RT0603BRD073KL
RES SMD 10R 1% 0.25W 1206	Chip Resistor 10R ±1% 0.25W 1206	R11, R12, R13	3	Rohm	KTR18EZPF10R0
RES SMD 220R 1% 0.125W 0805	Chip Resistor 220R ±1% 0.125W 0805	R17, R22	2	Yageo	RC0805FR-07220RL
ERJP06F15R0V	Chip Resistor Anti-Surge 15R ±1% 0.5W 0805	R18, R20, R24, R25	4	Panasonic	ERJP06F15R0V
ESR10EZPF49R9	Chip Resistor Anti-Surge 49.9R ±1% 0.4W 0805	R19, R23	2	Rohm	ESR10EZPF49R9
RES SMD 47k 1% 0.1W 0603	Chip Resistor 47k ±1% 0.1W 0603	R21, R26	2	Yageo	RC0603FR-0747KL
RES SMD 2.2k 1% 0.1W 0603	Chip Resistor 2.2k ±1% 0.1W 0603	R27, R39	2	Panasonic	ERA3AEB222V
UCR03EVPFLR470	RES 0.47 OHM 1% 1/5W 0603	R29, R30, R31, R32, R33, R34, R35, R36, R37, R38	10	Rohm	UCR03EVPFLR470
RES SMD 0R JUMPER 0603	Chip Resistor 0R Jumper 0603	R40	1	Multicomp	MC0603SAF0000T5E
RES SMD 0R Jumper 0805	Chip Resistor 0R Jumper 0805	R41, R42	2	Yageo	RC0805JR-070RL
RES SMD 100R 1% 0.1W 0603	Chip Resistor 100R ±1% 0.1W 0603	R43, R45, R50, R52	4	Yageo	RT0603FRE07100RL
RES SMD 220R 1% 0.1W 0603	Chip Resistor 220R ±1% 0.1W 0603	R44, R46	2	Yageo	RT0603FRE07220RL
RES SMD 15k 1% 0.1W 0603	Chip Resistor 15k ±1% 0.1W 0603	R47, R57	2	Yageo	RT0603BRD0715KL
RES SMD 4R7 1% 0.1W 0603	Chip Resistor 4R7 ±1% 0.1W 0603	R48, R49, R51, R53	4	Rohm	KTR03EZPF4R70
ERJUP6F10R0V	Chip Resistor Anti-Surge 10R ±1% 0.5W 0805	R54	1	Panasonic	ERJ-UP6F10R0V
U6982-CL	Transformer Push-Pull, 3.3-5V, SMT	T1, T2	2	Coilcraft	U6982-CLD
AP62301Z6-7	IC REG BUCK ADJ 3A 18Vin SOT-563	U1	1	Diodes	AP62301Z6-7
LDK320AM-R	IC REG LDO ADJ 0.2A SOT23-5	U2, U4	2	Diodes	AP2204K
74LVC2G14GV	Dual Schmitt Trigger Inverter, LVC	U3, U5	2	Nexperia	74LVC2G14GV,125

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Value	Description	Designator	Quantity	Manufacturer	Supplier P/N
SI8271AB-ISR	DGTL ISO 2.5KV GATE DRIVER 8SOIC	U6, U9	2	Silicon Labs	SI8271AB-ISR
74LVC2G86DC	DUAL 2-IN EX-OR GATE	U7, U8	2	Nexperia	74LVC2G86DC,125
74LVC2G08DC	Dual 2-Input AND	U10	1	Nexperia	74LVC2G08DC,125
74LVC1G74DC	74LVC Series 5.5 V SMT Single D-Type Flip-Flop; Positive-Edge Trigger - VSSOP-8	U11	1	Nexperia	74LVC1G74DC,125
74LVC1G14GW	Inverter Schmitt Trigger CMOS 5-Pin TSSOP	U12	1	Nexperia	74LVC1G14GW,125
SMA connector right angle	SMA Connector Right Angle PCB Jack 50Ohms	X1, X2	2	Molex	73391-0083
CONN HEADER VERT 3POS 2.54MM	Connector Header Through Hole 3 position 0.100" (2.54mm)	X3, X4	2	Wurth Electronics	61300311121
BNC PCB connector (Amphenol 112404)	CONN BNC RCPT STR 50 OHM PCB	X5	1	Amphenol Connex	112404
SMA connector straight	SMA Connector Straight PCB Jack 50Ohms	X7	1	Amphenol RF	901-144-8RFX
WE-746600330R	TERMINAL REDCUBE M3 SMD	X8, X9, X10, X11, X12, X13, X14	7	Wurth Electronics	746600330R
2-Pin Header 5.08mm vert green	Plug In Vertical To Pcb 2pos 12a 250vac Green Plastic Housing 5.08mm Pitch 5.08mm Length	X15	1	Wurth Electronics	691311500102
CONN HEADER VERT 2POS 2.54MM	Connector Header Through Hole 2 position 0.100" (2.54mm)	X16, X17	2	Wurth Electronics	61300211121
3-Pin Header 2.54mm lock	3 pin male Locking Header, THT, Vertical, pitch 2.54 mm, 1 x 3 position	X19	1	Wurth Electronics	61900311121
Cool Innovations 3-232312MFABLAN	Heatsink 60.00mm L X 60.00mm W X 30.48mm H	HS1	1	Cool Innvations	3-232312MFABLAN
Cooling Fan	60x60x15mm	Fan	1	Sunon	MF60151VX-1000U-A99
M4x20 Socket Head Cap Screw			8	Generic	
M4 Female-M4 Female 20mmThreaded standoff			4	Generic	

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Value	Description	Designator	Quantity	Manufacturer	Supplier P/N
M4 65mm Standoff	Wurth Elektronik Polyamide Hex Standoff, Male/Female 971650485, 65mm, M4		4	Wurth Electronics	971650485
M4 Nylon Nut			4	Generic	
M4 Nylon Washer			12	Generic	
Fan connector	Molex, KK 254 Female Connector Housing, 2.54mm Pitch, 4 Way, 1 Row		1	Molex	47054-1000
Fan Crimp Terminal	Molex, KK 254 Female Crimp Terminal 22AWG 08-50-0113		2	Molex	08-50-0113
Fan Guard	60mm x 60mm Metal Fan Guard		1	Generic	
M3x10 Pan Head	Pozidriv Pan Steel Machine Screws DIN 7985, M3x6mm		2	Generic	
M4x3mm Nylon Spacer	PCB Spacer, Round, Nylon 6.6, 6.3x3mm		4	Generic	
Alumina Shim	1L,ALN,40x40x0.6mm		1	SFX PCB	
X.210505 GAN039 TSC Double Pulse for Customer PCB	PCB		1	Wurth	
Inductor	Mag Inc 0078076A7 Core - 17 Turns 1.4mm Enamelled Copper Wire - M3 ring terminals	Fitted for Double Pulse (fitted as standard)	1	Amethyst Designs Ltd	
Inductor	Mag Inc 55439-A2 Core - 50 turns of 2.0mm # (AWG12 class 155C or higher) - M3 ring terminals	Fitted for Steady State Operation (not supplied)	0	Amethyst Designs Ltd	

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10. Revision history

Table 3. Revision history

Revision number	Date	Description
1.0	2024-01-09	Initial version.

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